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Dry-etched features for advanced waveguide design in GaN laser diodes

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Doctor of Philosophy
in
Electrical and Computer Engineering

by

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Curriculum Vitæ

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Education

2016	Ph.D. Electrical & Computer Engineering University of California, Santa Barbara
2011	M.Sc. Electrical & Computer Engineering University of California, Santa Barbara
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Experience

2012-16	University of California, Santa Barbara: Ph.D. program in Electrical & Computer Engineering (Solid State Lighting and Energy {Electronics} Center). Research on III-nitride laser diodes. Microchip fabrication, device simulation.
2011	Philips Lumileds Lighting Co.: Wafer Fab R&D — Engineering Intern. Project leader for Cu-deposition tool installation and qualification.
2009-11	University of California, Santa Barbara: Ph.D. program in Electrical & Computer Engineering. Research on IR/near-IR waveguides, PICs, and optical logic. Microchip fabrication, device simulation.
2007-09	University of Virginia: Research Experience for Undergraduates. Fabricated and tested organic solar cells, fabricated surface textured Si.
2006-07	Micron Technologies, Virginia: PVD Dept — Engineering Intern. Qualification and process control for metal thin films of Cu, Ta, WSi_x.

Awards

2015	Feature in "Highlights of 2015", *Journal of Semiconductor Science and Technology*
2009	University of California Graduate Opportunity Fellow
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Abstract

Dry-etched features for advanced waveguide design in GaN laser diodes

by

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Blue and violet laser diodes (LDs) made from the (Al,In)GaN material system were first demonstrated in 1995 and have since been commercialized for applications in data storage and display technology. As the material and device technology continues to mature, these laser diodes are being investigated for use in solid state lighting and wireless communications, most recently being utilized for high-end automobile headlights. Competitiveness in these markets will require new device designs of GaN-based LDs to improve the efficiency and optical output power.

A key structural element of a laser diode is the set of cladding layers around a waveguiding core which, together, confine the optical mode. This confinement is dependent on the refractive index contrast between the cladding and core. However, it is difficult to grow lattice-mismatched AlGaN and InGaN layers with high enough composition and thickness to provide the required index contrast. Therefore, research efforts have begun to explore new low index cladding options such as transparent conductive oxides and lattice-matched quaternary alloys.

In this work, I explore an alternative cladding design using etched nano-structures to lower the effective refractive index and create a high index-contrast top cladding layer. I present detailed simulations, design, and fabrication of blue (435.5 nm, 451 nm) laser diodes. I also consider the effect of sub-surface dry etch damage which can destroy the light emitting active region. While prior work on light emitting GaN nano-structures required GaN regrowths or recovery anneals, I have developed a low-

damage dry etch that avoids the etch damage issue. The resulting process is a new fabrication method for surface etched nano-structures in GaN light emitting devices.

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Chapter 1

Introduction & background

The design and fabrication of a finely patterned & etched waveguide cladding layer is carried out on the III-nitride material system for the purpose of improving the existing laser diode (LD) performance. Fundamentally, the concept of an etched cladding is not unique to III-nitrides or even to LDs. However, the advantages and disadvantages are measured within the context of III-nitride LDs, specifically around the blue wavelength (435 nm — 465 nm). The existing growth and fabrication challenges of the chosen device platform provide an opportunity, and thus a vehicle, to demonstrate this new fabrication technology. In doing so, the more general design concepts associated with an etched, high-index contrast cladding layer are developed.

Furthermore, the design and fabrication work presented leverages the wealth of knowledge on blue *m*-plane LDs that is present in the nitrides research group at the University of California, Santa Barbara (UCSB). [1–13] As such, this work will focus on addressing the platform-specific issues by developing a start-to-finish fabrication process. It is left to the reader to translate the developed design concepts and

fabrication processes to other devices and/or material systems.

1.1 Applications for blue III-nitride LDs

Currently, optical devices made from the III-nitride material system consist of GaN and its aluminum & indium alloys. The epitaxial layers — light emitting (active) region, waveguiding layers, and some or all of the cladding layers — are grown by metal organic chemical vapor deposition (MOCVD) at UCSB. The light emitting layers consist of InGaN quantum wells (QWs) that provide spontaneous and stimulated emission in the ultraviolet to yellow spectrum. [3] More importantly, the III-nitrides is currently the most efficient semiconductor material system for electroluminescence in the UV to green spectrum, making it essential for efficient lighting and display applications.

The band gap of GaN corresponds to the near UV wavelength, about 3.435 eV or 361 nm. Mixed with the larger band gap AlN (6.16 eV or 201.3 nm) or the smaller band gap InN (0.675 eV or 1837 nm) can produce light ranging from UV to IR, respectively. For instance, an InGaN/GaN LD with quantum wells (QWs) emitting blue light (450 nm) will have around 16% of the gallium lattice sites replaced by indium. The exact composition required is dependent on the QW geometry and orientation to the crystal plane.

Blue LDs have found a unique place in commercial devices for the purposes of lighting or display applications. Electrically injected blue LDs are an efficient way to produce high-power, collimated light from a small device, often the size of button when fully packaged. This light can then be used as is, or down-converted to other visible wavelengths before projection.

1.1.1 LDs for lighting and display

Lighting and display applications generally require the red-green-blue (RGB) primary colors to emulate white visible light. This is most often accomplished in one of two ways. The first method is to directly produce each of the RGB wavelengths separately and combine them at the output. The second method is to use a high energy wavelength like blue or UV and down convert some of light into the other visible wavelengths, with the end result approximating a white spectrum.

Down conversion is accomplished using phosphor materials. The phosphor cerium-doped yttrium aluminum garnet (Ce:YAG) down-converts near-UV to green wavelengths to a broad, yellow emission (FWHM $\sim 120\,\text{nm}$, peaked at $565\,\text{nm}$), absorbing most efficiently at blue ($425\,\text{nm}$ — $475\,\text{nm}$). [14, 15] Therefore, with just a blue light source and Ce:YAG, one can create a white visible light source.

Blue LDs for lighting has been well explored in research. [16] Blue LDs have the potential to overtake the commercially successfull LEDs (that use the same blue-pump/Ce:YAG down-conversion scheme), but would compete better if made more energy efficient. However, an LD does have an advantage when a small device package and directionality of emission are desired. With these benefits in mind, blue LDs entered the automobile market in 2014. [17] Lasers for lighting will have similar advantages in any application that requires a bright, directional beam such as a spot light.

Separately driven RGB(Y) lasers can also produce white light, [18] but are more useful in display applications. Reasonable power, size and efficiencies for the red and blue wavelengths have enabled small, palm-sized video projectors. [19] Currently, the green wavelength in these devices is produced by a frequency-doubled near-IR LD, at the cost of large footprint and poor efficiency compared to the other two wave-

lengths. With further development of III-nitride-based green LDs as replacements, these devices can shrink to much smaller dimensions.

1.1.2 Value-added laser lighting

Using the same principles of RGB LD display, RGB LED or LD lighting can bring a larger functionality to our everyday lighting. In particular, RGB lighting allows for the color to be tuned across the entire visible spectrum; for white lighting, the color temperature can be tuned "warmer" or "cooler". Adjusting the color temperature can help with regulating the human circadian rhythm — for instance, a cool white light ($\sim 2700\,\mathrm{K}$) gives our bodies cues to stay awake and alert compared to a warm, white light ($\sim 6500\,\mathrm{K}$). [3]

Another value-added use of laser lighting is visible light communications (VLC) using white light installations. With the spectral crunch of the currently used communications bandwidth, the unregulated visible spectrum is increasingly valuable for high-speed, large-volume, short-distance communications. [20]

A simple example of this technology is a blue LD pumping a phosphor to produce white light, but with a high-speed modulation ($\sim 4\,\mathrm{Gbps}$) of the LD to transmit data. [21] The achievable data rates are many orders of magnitude larger than current Wi-Fi standards. The pump laser modulation rate is much too fast to be observed by the human eye as well as being much faster than the relaxation time of Ce:YAG phosphors. With a proper DC-balanced encoding scheme, the white lighting functionality will be virtually unchanged while providing excellent line-of-sight communications.

1.2 The III-nitride material system

For this work, the bulk GaN, non-polar *m*-plane substrate (supplied by the Mitsubishi Chemical Corporation) was chosen as the test platform. Even though this crystal plane has been well-developed at UCSB, there are still areas that can be improved. Therefore, it serves as a good demonstration vehicle for new LD design geometries.

1.2.1 Substrates and epitaxial growth

The waveguiding layers surrounding the light emitting QWs typically consist of GaN or lower indium content $In_xGa_{1-x}N$. The outer cladding layers are lower refractive index materials like GaN, AlGaN, or material deposited during microfabrication. Often times an electron blocking layer of AlGaN is grown on the p-side of the active region to better confine electrons, but to the slight detriment of the optical mode profile. A detailed look at the optical properties of $(Al_x,In_x)Ga_{1-x}N$ materials is presented in *Appx. A*.

Together, these layers form a waveguide to direct light emission, confining the light vertically around the QWs. For electrically pumped devices, these layers must also form a p-i-n diode via p-type and n-type dopants. During GaN growth by MOCVD, the magnesium p-type dopant must be at the top of the epitaxial growth. This constraint is because the as-grown Mg-doped GaN is not conductive until an atmospheric anneal at $\geq 600\,^{\circ}C$ drives the hydrogen impurities out through the surface. [22] This hydrogen diffusion is blocked by n-type material. Therefore, the junction orientation is fixed, with p-type material above the active region (extending to the surface), and Si-doped n-type material below.

These epitaxial structures are most often grown on either bulk GaN substrates or sapphire substrates, and on a variety of crystal planes. The current industry standard is to grow the *c*-plane orientation on 6 in. or 8 in. diameter single-crystal sapphire substrates. Using large wafers lowers the per-device cost, but the strained heteroepitaxy of GaN on sapphire produces $3 \times 10^8\,\mathrm{cm}^{-2}$ threading dislocations [23] that will reduce the efficiency of light generation. Advanced growth techniques like lateral epitaxial overgrowth can stifle the propagation of threading dislocations in localized areas. [24]

Alternatively, one can use bulk GaN substrates for low dislocation density ($5 \times 10^6\,\mathrm{cm}^{-2}$) growth. [25] Currently, bulk substrates are limited to 2 in. diameter wafers for the maximally polarized, basal *c*-plane and only $\sim 6\,\mathrm{mm} \times 12\,\mathrm{mm}$ wafers for the (nearly) perpendicular-to-*c*-plane planes of non-polar and semi-polar (NP/SP). Laser diodes on NP/SP substrates will only be commercially viable competitors to *c*-plane GaN if they can be made on larger surface area substrates.

1.2.2 Consequences of heteroepitaxy on waveguide design

Due to the polar nature of the GaN unit cell, heterojunctions of (Al,In)GaN layers produce a substantial polarization charge in the **c**-direction. Fundamentally, the reduced polarization of NP/SP substrates promises better LD device performance than *c*-plane. [3] Unfortunately, the critical thickness on NP/SP substrates is lower and the impurity concentration is higher. Recently at UCSB, great strides toward high power continuous-wave blue LDs have been made on the $(20\bar{2}\bar{1})$ plane, [26] but have yet to prove better performance than industry *c*-plane devices.

Only GaN and the ternary alloys of $Al_xGa_{1-x}N$ & $In_xGa_{1-x}N$ are used in this work. The quaternary $Al_xIn_yGa_{1-x-y}N$ is not used for optical devices at UCSB, simply

because the growth space and material properties are not well explored. The result is that all of the heteroepitaxial layers are lattice-mismatched and under tremendous strain.

The mismatch to GaN trends with alloy content, with $Al_xGa_{1-x}N$ under tensile strain and $In_xGa_{1-x}N$ under compressive strain. This strain restricts the thickness of heteroepitaxial layers, restricting general laser diode design. If the critical thickness is exceeded, catastrophic breakdown of the surface morphology will ruin device performance. [27]

The restriction of alloy amount & thickness drives a lot of the waveguide design. Without the ability to grow thick, high-index contrast layers, this work focuses on a fabrication approach as a substitute for the top waveguide cladding. However, the resulting etched cladding is not necessarily in competition with other cladding options, but can be integrated together if desired.

1.3 Fabrication challenges for III-nitride LDs

Besides the growth restrictions imposed by the ternary heteroepitaxy, the GaN-based material system has two major areas of difficulty for LD device design. First, the only known p-type dopant is the deep acceptor, magnesium-vacancy complex. Because of its low ionization ratio of $\sim 1\%$, [28] $100\times$ more Mg is required to dope a bulk (Al,In)GaN layer p-type than the desired carrier density.

Second, GaN is very resistant to chemical etching, leaving few etching options. In fact, using standard photoresist masks, there is no acceptable wet etch to transfer a lithographic pattern into GaN. [29] Therefore, dry etch is the only etch method to shape the as-grown waveguide into the desired LD device geometry.

1.3.1 Difficulties with Mg-doped GaN

Fabrication with an exposed surface of Mg-doped GaN is very restricted. It has been previously observed that any plasma exposure compensates the doping, leading to highly resistive electrical contacts. [30, 31] Therefore, the p-GaN surface must be protected before any plasma deposition or etch can be performed. Usually, this protection layer is not the electrical contact layer, so it must later be removed to make contact. A functional fabrication process must accommodate these restrictions.

To make an ohmic contact, a top layer of highly doped p-GaN ($[\mathrm{Mg}] \cong 10^{20}\,\mathrm{cm}^{-3}$) is required. This layer is very optically lossy (see *Appx. A*), simply due to the presence of the vast quantity of unionized dopant. [32] To avoid these optical losses, the contact layers must either be far away from the waveguide core, or be optically blocked by a distinct cladding layer. With the limited epitaxy options described above, many LD device designs on NP/SP use a thick p-GaN layer of 700 nm or more.

1.3.2 Etching options for (Al,In)GaN

The GaN material system is very resistant to both wet etch and dry etch chemistries. For wet etching, hot ($> 100\,^{\circ}\mathrm{C}$) solutions of KOH or H_3PO_4 have been found to etch GaN crystallographically, etching the *m*-plane the fastest while leaving the *c*-plane untouched. [33] They have been used to create surface roughening for light emitting diodes (LEDs), [34, 35] but have not been successful in transferring lithographically defined patterns.

For anisotropic transfer of a lithographic pattern, halogen-based chemistries have proven successful. [36] Chlorine-based dry etches are the most common, using either Cl_2, BCl_3, or $SiCl_4$ as the carrier for the reactive species, and H_2, N_2, or Ar as the

plasma-enhancing species. [37]

Fluorine-based dry etches typically use SF_6 as reactive species source. This dry etch is useful when etch selectivity between (In)GaN and AlGaN is needed — the fluorine bonds to Al forming AlF_x, which is much less volatile than the other etch products and therefore retards etching. [38] In general, the (Al,In,Ga)F_x compounds are much less volatile than (Al,In,Ga)Cl_x compounds, so etch rates will be slower.

In this work, we will focus on a Cl_2/Ar-based dry etch in order to lithographically pattern GaN. This chemistry shows high etch rates [39] and has been previously used to fabricate *m*-plane GaN LD devices.

1.4 Dissertation overview

A new cladding layer consisting of alternating etched and un-etched stripes of GaN is fabricated as part of an advanced waveguide design for GaN LD devices. This cladding layer is dubbed an "etched-gap cladding" (EGC), or more specifically an "air-gap cladding" (AGC) if the etched trenches are left unfilled and capped.

This new approach to GaN LD device design is first simulated with various 1-D and 2-D techniques. Supporting these simulations is a cohesive collection of material parameters. The simulations provide both an initial design and analysis tool for the fabricated devices.

During fabrication of AGC- and EGC-LDs, a number of new fabrication steps were developed. A new low-damage dry etch was developed and experimentally verified for use near layers sensitive to mid-gap defects, e.g. light-emitting QWs. An electron-beam lithography process was developed for low line-edge-roughness features. More process steps were developed to provide a start-to-finish fabrication process for EGC-LDs.

1.4.1 Simulation of III-nitride waveguides

Optical simulation of III-nitride waveguides begins with a good foundation of the optical material parameters. *Appx. A* provides a cohesive model for the band gap energy, refractive index, and absorption for GaN, AlGaN, and InGaN.

Using these material parameters, the transfer matrix method (TMM, *Appx. C*) is applied to different III-nitride waveguide designs implemented using the MATLAB® code platform. [40] A simple model for the effective index of the EGC layer (*Appx. B*) is incorporated into TMM so that simulated 1-D optical modes can be investigated. The 1-D optical mode simulations are then compared to 2-D mode simulations using the commercial software FimmWave. [41]

1.4.2 Design and fabrication of a new cladding layer

Using simulation, the geometry of an etched gap cladding was laid out. A fill-factor of 50% and a pattern period of 300 nm produces a layer that optically performs nearly identical to a uniform layer of much lower index. The next step was to reproduce the simulated geometry through microfabrication processes at the Nanofabrication Facility at UCSB.

The fabrication of this geometry hinged on two important aspects: first, the EGC had to be close enough to the optical mode to affect it. Since a laser mode is generally centered on the light-emitting QWs, this means that the dry etch to create the EGC comes dangerously close to the QWs. To prevent detrimental defect formation, a new, low-damage dry etch was developed and thoroughly tested.

Second, the EGC had to be patterned and etched at the small scale of a 300 nm period. To this end, a holography process and a new electron beam lithography

process were developed for use on GaN.

1.4.3 LD device demonstrations

The end result of device simulation and process development was two generations of etched-gap clad laser diodes. The 1st generation is a simpler design, utilizing a metal capping technique to leave air-holes, resulting in an AGC-LD. These LD devices lased at 435.5 nm at room temperature under pulsed electrical injection.

The 2nd generation of EGC-LDs leveraged the learning from the 1st generation and a new electron beam lithography process to allow for both EGC-LD and standard ridge LD devices on the same substrate. An electrical shorting issue was discovered across the pn-junction of the LDs. Detailed failure analysis points to a single process step and not to the EGC layer. Regardless, only a select few of the ridge LD devices lased under pulsed electrical injection, but none of the EGC-LDs lased.

The simulation, process development, and device demonstration of EGC-LDs set the stage for new LD device designs. In addition, the unique processing tools developed allow more flexibility for in designing future III-nitride optoelectronic and electronic devices.

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Chapter 2

(Al,In)GaN waveguide simulation

The geometry & refractive index of the constituent layers that comprise the $(Al_x,In_x)Ga_{1-x}N$ LD will determine the shape of the supported optical modes. In non-magnetic media (i.e. the relative magnetic permeability, μ_r, is unity) as we most often have in GaN waveguides, this electromagnetic (EM) wave can be uniquely characterized by the electric phasor profile at a 2-D cross-sectional plane of the waveguide. The implied time-varying factor $e^{i\omega t}$ is determined by the chosen wavelength. We also assume that the waveguide geometry is invariant in the dimension perpendicular to the chosen 2-D cross-sectional plane.

The interaction of the complex electric field with the volume of material can tell us what some of the external characteristics of the LD mode will be. Specifically, the overlap of the electric field with each volumetric feature of the waveguide can tell us the confinement factor of each feature and thus the resulting absorption, gain, or scattering of the mode.

By using a variety of semi-analytical and numerical techniques, we can simulate

these modes and inspect the resulting internal LD characteristics. The accuracy of our simulation and the determined internal LD characteristics are subject to the assumptions we make in regards to material parameters, spatial symmetry, and boundary conditions. For all of the following simulations, n, the refractive index and α, the absorption (collectively, the complex refractive index, $\tilde{n}$) of various materials used are provided in *Appx. A*.

For the entirety of this work, we will restrict ourselves to in-plane waveguides, meaning that the power flow of the modes is parallel to the growth surface. Furthermore, we will most often consider TE(-like) modes, meaning the electric field of the EM wave oscillates *nearly* perpendicular to the power flow. In slab-like waveguides (e.g. ridge waveguides) that contain epitaxially grown quantum wells (QWs), the electric field is approximately parallel to the growth surface and planes of QWs — for 1-D slab waveguides, it is exactly so. We assume TE modes simply because QWs exhibit higher gain for TE modes; [1] thus, in-plane laser modes of interest are all TE polarized.

2.1 Methods for simulations of optical modes

In this work, we use two different techniques to simulate optical waveguides: the Transfer Matrix Method (TMM) and Film Mode Matching (FMM). In both cases, we must start with the electromagnetic properties of the constituent materials derived from free-space constants, so the following definitions are provided:

Table 2.1: Electromagnetic constants for free-space and material properties.

Property	Free-Space Constant	Free-Space Value	Material Property
Permittivity	ε_o	$8.854 \times 10^{-12}\,\mathrm{F/m}$	$\varepsilon = \varepsilon_\mathrm{o}\varepsilon_r$
Permeability	μ_o	$1.257 \times 10^{-6}\,\mathrm{H/m}$	$\mu = \mu_\mathrm{o}\mu_r \approx \mu_\mathrm{o}$
Speed of light	$c_\mathrm{o} = 1/\sqrt{\varepsilon_\mathrm{o}\mu_\mathrm{o}}$	$2.998 \times 10^{8}\,\mathrm{m/s}$	$c \approx c_\mathrm{o}/\,\mathrm{Re}(\sqrt{\varepsilon_r})$
Wave impedence	$\eta_\mathrm{o} = \sqrt{\mu_\mathrm{o}/\varepsilon_\mathrm{o}}$	$376.3\,\Omega$	TE: $\eta = \eta_\mathrm{o}/\sqrt{\varepsilon_\mathrm{o}}$ TM: $\eta = \eta_\mathrm{o}\sqrt{\varepsilon_\mathrm{o}}$
Wavelength	λ_o	user-defined, e.g. 450 nm	$\lambda = \lambda_\mathrm{o}/\,\mathrm{Re}(\sqrt{\varepsilon_r})$
Wavenumber	$k_\mathrm{o} = \dfrac{2\pi}{\lambda_\mathrm{o}}$	user-defined, e.g. 13.96 µm	$k = k_\mathrm{o}\sqrt{\varepsilon_r}$

Table 2.2: Definitions of material and modal properties.

Property	Constant
Dielectric constant	$\varepsilon_r = \tilde{n}^2$
Refractive index	$\tilde{n} = n + i\kappa$
Modal effective index	$\tilde{n} \to \tilde{n}_\mathrm{eff}$
Absorption (or gain[1])	$\alpha = \dfrac{4\pi\kappa_\mathrm{eff}}{\lambda_\mathrm{o}}$
Propagation constant	$\beta = \dfrac{2\pi n_\mathrm{eff}}{\lambda_\mathrm{o}}$
Wavenumber	$k = \dfrac{2\pi\tilde{n}_\mathrm{eff}}{\lambda_\mathrm{o}} = \beta + i\dfrac{\alpha}{2}$

[1]Material gain, $g = -\alpha$, occurs when κ is negative instead of positive

2.1.1 Transfer Matrix Method — MATLAB®

TMM is used to view the effect of epitaxial layers and vertical geometry on the supported modes. It is implemented using code written with the MATLAB [2] platform (*Appx. C*) to quickly return a 1-D profile of the mode(s) based on the refractive index ($\tilde{n}$) and thickness of each layer (Fig. 2.1). For a TE mode, the computational program finds the electrical field such that the field intensity transmitted from the top to the bottom is minimal. The TM modes can be found in a similar fashion, but the program must evaluate the transmission of the magnetic field instead. The resulting standing-wave profile is a mode. Its unique propagation constant can be characterized by an "effective" refractive index, $\tilde{n}_{\text{eff}}$.

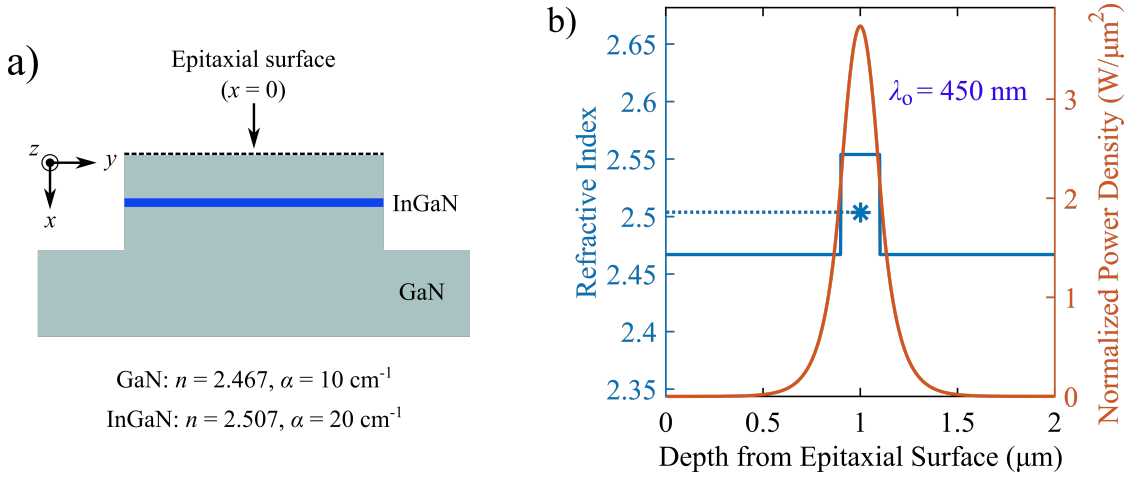

Figure 2.1: **a)** Schematic cross-section of an $In_xGa_{1-x}N$/GaN waveguide. **b)** Time-averaged power density for the 1-D mode profile (TE, fundamental mode) with assumed material properties and thicknesses of (*a*) — the refractive index profile is given (blue line) and the effective index of the mode is indicated (dashed orange line). Note that the integrated power is 1 W for a 1 µm-wide slice of waveguide in the *y*-direction.

Table 2.3: Formulae for TE(-like) & TM(-like) modes of a slab(ridge) waveguide.

Field	TE Formula	TM Formula	SI Unit
Electric field	$\boldsymbol{E} = E_x\hat{\boldsymbol{x}} + E_y\hat{\boldsymbol{y}} + E_z\hat{\boldsymbol{z}}$		V/m
	$E_x = 0$	$E_x = \frac{\tilde{n}_{\text{eff}}\eta_{\text{o}}}{\tilde{n}^2}H_y$	
	$\boldsymbol{E} = E_y\hat{\boldsymbol{y}}$	$E_y = 0$	
	$E_z = 0$	$E_z = \frac{j\eta_{\text{o}}}{\tilde{n}^2 k_{\text{o}}}\frac{\partial H_y}{\partial x}$	
Electric flux	$\boldsymbol{D} = \tilde{n}^2\varepsilon_{\text{o}}\boldsymbol{E}$		A·s/m^2
Magnetic field	$\boldsymbol{H} = H_x\hat{\boldsymbol{x}} + H_y\hat{\boldsymbol{y}} + H_z\hat{\boldsymbol{z}}$		A/m
	$H_x = \frac{\tilde{n}_{\text{eff}}}{\eta_{\text{o}}}E_y$	$H_x = 0$	
	$H_y = 0$	$\boldsymbol{H} = H_y\hat{\boldsymbol{y}}$	
	$H_z = -\frac{j}{k_{\text{o}}\eta_{\text{o}}}\frac{\delta E_y}{\delta x}$	$H_z = 0$	
Magnetic flux	$B = \mu_{\text{o}}\boldsymbol{H}$		V·s/m^2
Electric power density	$I_{\text{E}} = \frac{n}{2\eta_{\text{o}}}\lvert\boldsymbol{E}\rvert^2$		W/m^2
	$= \frac{n}{2\eta_{\text{o}}}\lvert E_y\rvert^2$	$\approx \frac{n_{\text{eff}}^2\eta_{\text{o}}}{2n^3}\lvert H_y\rvert^2$	
Time-avg. power flux	$\langle\boldsymbol{S}\rangle = \frac{1}{2}\boldsymbol{E}\times\boldsymbol{H}^*$		W/m^2
	$\approx \frac{n_{\text{eff}}}{2\eta_{\text{o}}}\lvert E_y\rvert^2\hat{\boldsymbol{z}}$	$\approx \frac{n_{\text{eff}}\eta_{\text{o}}}{2n^2}\lvert H_y\rvert^2\hat{\boldsymbol{z}}$	

The coordinate axes of Fig. 2.1.a will be the standard used in this work. In particular, note that the x-axis points downwards when looking at a standard ridge cross-section. This is done so that the field profile can be displayed with axis label depth from epitaxial surface implying that the grown surface is the zero of the x-axis.

The program iteratively checks the solution(s) to the eigenvalue problem. A range of trial $\tilde{n}_{\text{eff}}$ are input into the matrix and checked. The vertical electric field profile is the eigenmode and $\tilde{n}_{\text{eff}}$ is the eigenvalue. Thus, it is a semi-analytical technique. For TE modes ($\boldsymbol{E} = E_y\hat{\boldsymbol{y}}$), the other field profiles are determined from the electric field profile, assuming that $\boldsymbol{E}$, n, and κ are functions of y, while TM modes ($\boldsymbol{H} = H_y\hat{\boldsymbol{y}}$) are determined from the magnetic field profile (Table 2.3).

In general, the quantities $\boldsymbol{E}$, $\boldsymbol{D}$, $\boldsymbol{B}$, and $\boldsymbol{H}$ are complex vector fields, along with the wavevector $\boldsymbol{k}$. Each vector component (e.g. E_x, E_y, or E_z) is itself a function of x, y, and z. For TE modes, vector fields $\boldsymbol{E}$ and $\boldsymbol{D}$ only have y-components while the vector fields $\boldsymbol{B}$ and $\boldsymbol{H}$ have x-components as well as z-components that are dependent on the mode profile in the x-direction. Table 2.3 details how to derive many of the important EM quantities for a mode using the x-dependent material properties ($n(x)$, $k(x)$) and eigenmode ($E_y(x)$, or $H_y(x)$), and the eigenvalue ($\tilde{n}_{\text{eff}}$). The imaginary part of the eigenvalue (κ_{eff}) also determines the modal loss.

The quantity $\boldsymbol{S}$ is also known as the Poynting vector. It represents the power flow of the mode as it travels the transverse axis of the waveguide, and thus the vector only has a z-component. The time-averaged quantity, $\langle\boldsymbol{S}\rangle$,varies in the xy-plane, but will not vary in the z-direction as long as the waveguide is uniform in z.

The electric field is normalized such that the integrated $\langle\boldsymbol{S}\rangle$ is unity. Now, the confinement factor, Γ, of each layer, i, is given by [3]:

$$\Gamma_i = \frac{\int_{L_i} I_{\text{E}}(x)\,dx}{\int_{\infty} \left(\langle\boldsymbol{S}(x)\rangle\cdot\hat{\boldsymbol{z}}\right) dx} \Rightarrow \int_{L_i} I_{\text{E}}(x)\,dx \tag{2.1}$$

This quantity represents the electric power experienced by a layer per unit of total power flow.[2] It is *not* the fraction of power in each layer (the sum of all layer confinement factors will not be unity). This becomes clear if we expand the numerator and denominator of Eq. 2.1:

$$\Gamma_i = \frac{\int_{L_i} I_{\mathrm{E}}(x)\,dx}{\int_{\infty} \left(\langle \boldsymbol{S}(x)\rangle \cdot \hat{\boldsymbol{z}}\right) dx} = \frac{n_i}{n_{\mathrm{eff}}} \frac{\int_{L_i} \left|E_y(x)\right|^2 dx}{\int_{\infty} \left|E_y(x)\right|^2 dx} \tag{2.2}$$

Thus, Γ_i consists of a fractional overlap (which *would* sum to unity over all layers) multiplied by the factor n_i/n_{eff} (or the factor n_{eff}/n_i for a TM mode). However, Γ_i is still referred to as the fractional overlap itself and reported as a percentage.

Since all interactions with a (non-magnetic) material occur through the electric field, the power gain coefficient (or absorption coefficient) of each layer can be directly calculated by multiplying Γ with the material gain (or material absorption):

$$G = \prod_i e^{\Gamma_i g_i l} \tag{2.3}$$

where G is the power gain over a distance l, and g_i is the material gain (or α_i for material absorption) of layer i.

The fractional overlap is calculated numerical. The accuracy is dependent on how accurately the eigenmode and eigenvalue are found as well as how fine a vertical grid is chosen for numerical integration. The fractional overlap multiplied by the material absorption over all layers (i.e. total modal absorption) can be directly compared to the imaginary part of the eigenvalue as a quick measure of accuracy.

The TMM assumes the 3-D waveguide acts as a 1-D slab with layers defined in the x- (vertical) dimension and extending infinitely in the yz-plane. While it is accurate

[2]Note that this is the vertical confinement factor, Γ_x. The full accounting is $\Gamma = \Gamma_x\Gamma_y\Gamma_z$. However, Γ_y is assumed to be unity for a slab-like waveguide, and Γ_z is assumed to be unity for sufficiently long in-plane waveguides.

in determining the supported slab modes, a waveguide that is highly confined in the y- (lateral) or z- (transverse) dimension will deviate from the slab mode. There is also an inherent assumption that each layer is uniform in the yz-plane. If this is not the case, an effective medium with an effective index must be used in place of the non-uniform layer (see *Appx. B*). Then, the assumption is that the size of the non-uniformities in the replaced layer is smaller than the wavelength of light in each of the constituent materials and generally has a consistent ratio of constituent materials.

TMM is also subject to boundary conditions at the top and bottom of the vertical dimension. However, since this method is quick and uses minimal computer resources, the full epitaxial growth including the substrate and a few metal layers can be simulated if necessary. Therefore, it is not susceptible to spurious results due to imposed non-physical boundary conditions and can handle large vertical modes that propagate into a thick substrate (e.g. leaky modes — §2.2.3).

2.1.2 Film Mode Matching — FIMMWAVE®

The FMM method, also called Eigenmode Expansion (EME), is well suited to solving well-behaved (e.g. non-leaky) 2-D optical modes in the xy-plane. It requires that the constituent geometries be rectangles of optically-defined material (represented by their complex refractive index) so that the linear system is locally separable into x- and y-components. Inherent in a 2-D solution is the assumption that the remaining z- (transverse) direction is uniform. Due to the semi-analytical nature that is very similar to TMM, a large number of layers can be represented in the vertical dimension to find the eigenvalue solutions with minimal computational overhead. In simple LDs, this is the situation of interest.

For 2-D simulations, we use the commercial software FIMMWAVE [4] that em-

ploys the FMM technique. Like TMM, the imaginary part of the complex eigenvalue can be checked against the fractional overlap multiplied by the material absorptions to see that the required level of accuracy has been achieved.

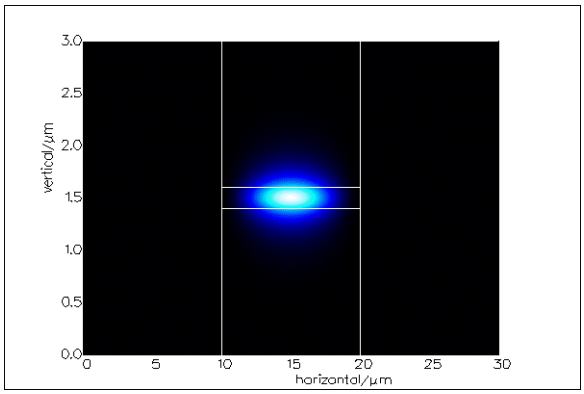

Figure 2.2: FIMMWAVE simulation — heat map of the fundamental mode power flux (transverse direction) of a 2-D waveguide. The materials and thicknesses are the same as those of Fig. 2.1.

Table 2.4: Comparison of 1-D (Fig. 2.1) and 2-D (Fig. 2.2) mode profile simulation results. The 2-D (*v2*) is calculated with a higher precision than the 2-D (*v1*).

Parameter	1-D	2-D (*v1*)	2-D (*v2*)
n_{eff}	2.4775	2.4774	2.4774
κ (10^{-5})	5.18	5.18	5.18
α_{EV} (cm^{-1})	14.472	14.465	14.465
α_{Ov} (cm^{-1})	14.471	14.443	14.463
Γ_{InGaN}	44.42%	44.14%	44.34%

In the above figure, the fundamental mode of a deeply etched (SiO_2 ridge cladding) waveguide is shown. Isolating the ridge laterally so that it has a uniform boundaries results in a mode shape that is separable in x and y and increases its similarity to a

slab mode. A relatively large ridge width (10 µm) was also chosen so that the mode behaves similarly to a 1-D slab mode.

We mainly use FIMMWAVE as a check of 1-D simulations by comparing modal effective indices, mode shapes, and layer absorption, especially in the cases of highly laterally-confined waveguides (see §2.2.1). Table 2.4 shows how similar the results are between a 1-D structure and a similar 2-D structure that is *not* well confined laterally. In this case, we are only considering the fundamental (lateral) mode of a waveguide that has many lateral modes. Note that two different 2-D simulationa are compared – the difference between them is that the second version (/textitv2) numerically calculates the fractional overlaps with an order of magnitude greater precision in both dimensions: 900 grid points in the lateral dimension and 1200 gridpoints in the vertical dimension.[3]

FIMMWAVE simulations are also used to check the validity of the effective medium assumptions. When these assumptions start to break down, we can see that the corresponding size of the structures in the layer are large and cause the mode shape to deform from the intended design (see §2.2.2).

The boundary conditions for this 2-D simulation are more stringent than the 1-D case. Because the simulation takes more computational resources, the cross-sectional area is limited to $\sim 500\lambda$ laterally and $\sim 50\lambda$ vertically for common in-plane waveguide geometries. Note that the typical waveguide will consist of a few repeated slices laterally, while each slice may be made up of hundreds of thin layers vertically. Symmetry in either direction can be leveraged so that only half the simulation area

[3]Proceeding, all FIMMWAVE simulations will be run with the following solver engine settings: 300 1-D modes and 900 × 1200 grid points. Solving for 300 1-D modes requires intermediate "polishing" steps of 30 and 100 beforehand, in order to compute in a timely manner. After finding the eigenmode(s), the fine grid is applied.

needs to be considered; most waveguides will be horizontally symmetric.

The four boundaries in the xy-plane must be set to the non-physical states of a perfect electrical reflector (perfect metal) or a perfect magnetic reflector. Thus, the mode must be well-behaved — it must be fully contained with its evanescent fields dropping to negligible values at the boundaries, otherwise non-physical solutions will result. Perfectly matched layers (PMLs) that artificially absorb energy can be added to the left and right hand side boundaries to negate spurious lateral modes. [5] Sometimes it will not be clear that the answer is non-physical, as seen with a vertically leaky mode (see §2.2.3).

2.2 Mode profile simulations of InGaN/GaN waveguides

We now apply the simulation techniques discussed so far, the optical properties defined in *Appx. A*, and approximations of *Appx. B* in order to view the optical mode in a typical $In_xGa_{1-x}N$/GaN ridge LDs (RDG-LD). We then introduce a surface etched structure at the top of the optical mode called an Etch Gap Cladding (EGC-LD).

2.2.1 Simulations of basic waveguides

We compare the 1-D and 2-D mode profiles of a GaN-$In_xGa_{1-x}N$-GaN waveguide at $\lambda_o = 450\,\text{nm}$. We continue with the material properties and epitaxial thicknesses of Fig. 2.1 and look at 2-D waveguide cross-sections. Now we consider shallow ridge designs where we etch a ridge to the InGaN layer and back-fill with SiO_2 once again.

Fig. 2.3 shows how a shallow ridge confines the lateral dimension of the mode even

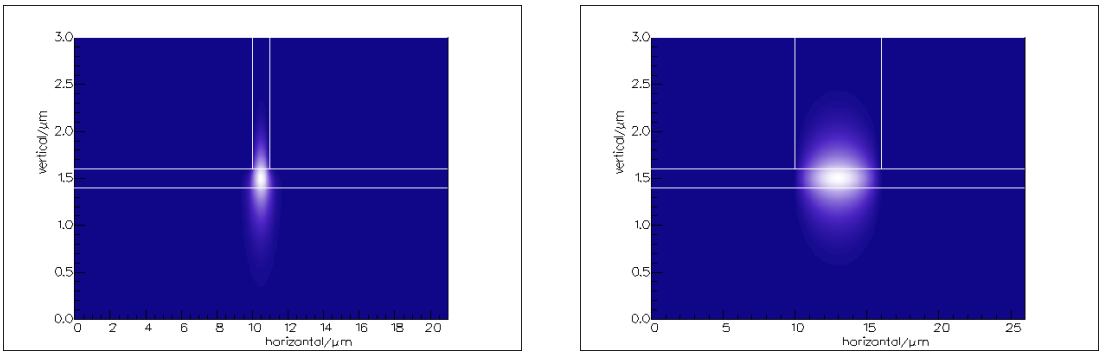

Figure 2.3: Mode intensity of shallow ridge waveguides of 1 µm width (*left*) and 6 µm width (*right*). Material properties are the same as for Fig. 2.1.

though the mode extends below the ridge. However, the mode shape will start to bend into a bottom-heavy T-shape, causing both the confinement factor and absorption to deviate from a 1-D slab mode or wide-ridge mode. A summary is provided below.

Table 2.5: Comparison of the waveguide geometries in Fig. 2.1, Fig. 2.2, and Fig. 2.3.

Parameter	1 µm Shallow RDG	6 µm Shallow RDG	10 µm Deep RDG	(1-D) Slab
n_{eff}	2.4716	2.4772	2.4774	2.4775
κ (10^{-5})	5.10	5.18	5.18	5.18
α_{EV} (cm^{-1})	14.250	14.465	14.465	14.472
α_{Ov} (cm^{-1})	14.245	14.464	14.463	14.471
Γ_{InGaN}	39.27%	44.32%	44.34%	44.42%
Eff. Area (μm^2)	0.72	2.85	4.56	N/A

Despite the narrow lateral confinement of the 1 µm-wide shallow ridge, there is very little variation in refractive index, total loss calculation, or the confinement factor of the center $\text{In}_x\text{Ga}_{1-x}\text{N}$ layer. Therefore, the 1-D simulation is taken as a good estimate of a (shallow or deep) ridge waveguide mode in general.

2.2.2 The effective medium layer

In this work, we will use an effective medium as a low index cladding layer for $In_xGa_{1-x}N$/GaN waveguides. The effective medium is created by etching a periodic tooth-trench geometry into the epitaxial surface, parallel to the transverse direction of the waveguide. The xy-cross-section remains uniform in the transverse direction, allowing an accurate depiction of the waveguide using FIMMWAVE:

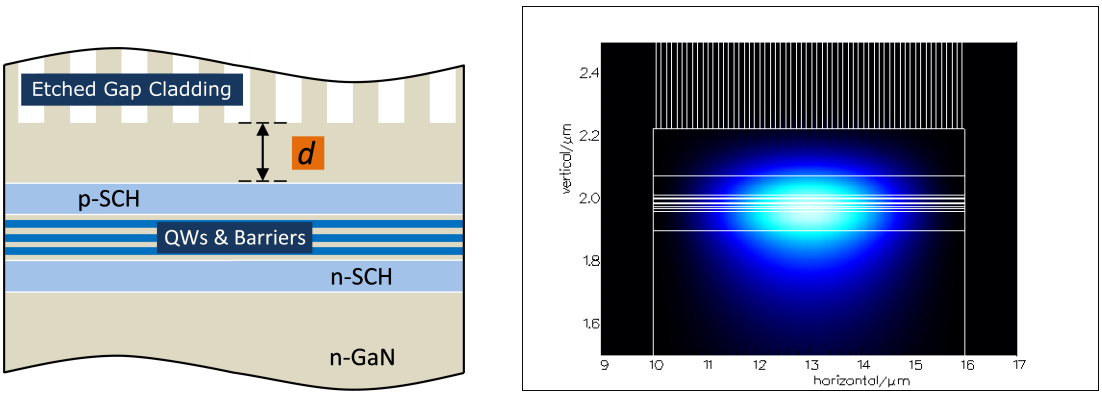

Figure 2.4: *Left:* Schematic cross-section of an EGC-LD (2^{nd} generation LDs). The trenches are etched a distance d away from the p-doped waveguiding layer. *Right:* A 2-D simulation of a deep ridge waveguide with an EGC: $d = 150\,\text{nm}$; $\lambda = 451\,\text{nm}$; fundamental mode only.

Fig. 2.4 shows the schematic and 2-D simulation of a grown and processed 6 µm-wide deep ridge EGC-LD, given in §5.2. The current feature of interest is the shape of the mode in the top EGC layer: as the EGC is changed, the mode shape will also change. We can use the confinement factor of this layer as a measure of how much the mode shape changes. Now, we can compare Γ_{EGC} while changing the tooth & gap widths, keeping both the ridge width (6 µm) and tooth/trench fill fraction (50/50) the same:

Using the Bergmann EMA from *Appx. B*, we can replace the EGC with its TE

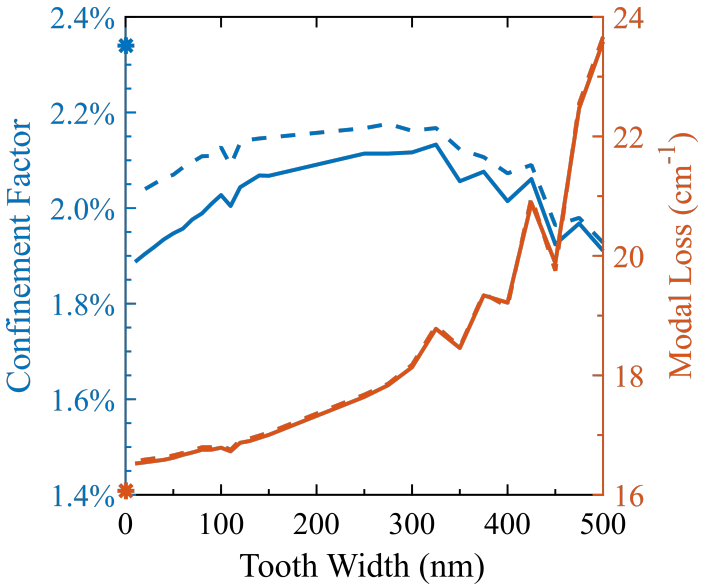

Figure 2.5: Confinement factor and modal loss in AGC-LD (1st generation LDs) vs. AGC tooth & trench width. For this structure, the mode shape is deviates sharply from the EMA at a tooth width of 300 nm. The dashed lines represent a deeply etched structure and shows less deviation from the 1-D EMA simulation (starred points).

approximation. Therefore, we replace the EGC layer with on that has $n_{\text{EMA}} = 1/\sqrt{(1-ff)/n_{\text{GaN}}^2 + ff/n_{\text{fill}}^2}$, where the ff is the fill fraction and the fill material is BCB. From Fig. 2.5, we see that the EMA simulation is a good approximation until the tooth & trench width is approximately 300 nm. This upper bound is dependent on the ridge geometry and the free-space wavelength. Since we will be using similar structures, we assume the EMA replacing a tooth & width of 150 nm is acceptable for this work.

The EMA allows us to reduce the 2-D EGC structure into a 1-D layer. Using this 1-D layer, we can create an equivalent 1-D model with the TMM. It allows for an extra degree of freedom over FMM: we can now represent a variable tooth/trench fill fraction. Therefore, we also simulate a triangular shape trench (150 nm deep) that better represents a fabricated structure. With FMM, such a feature would need to be

discretized into rectangle-based staircase geometry, and the computational overhead would be prohibitive.

2.2.3 Comparing 1-D vs. 2-D simulations: leaky modes

Now that we have the ability to approximate a 2-D waveguide cross-section as a 1-D slab mode, we can explore more detail in the vertical dimension. First, as mentioned previously, we can represent the triangular-shaped etched trench by varying the fill factor in the vertical dimension. We can also more faithfully represent the epitaxial layers. For instance, a superlattice of many repeated epitaxial layers are easily handled in the 1-D TMM solver, but are often approximated as a single layer in the FIMMWAVE solver to speed up the computation.

In rare cases, the full height of the epitaxial substrate must be simulated to faithfully recreate modal parameters. The substrate is often quite thick compared to the grown epitaxial layers: while a QW may only be a few nm thick, the as-received m-plane substrate is approximately 300 µm thick, a difference of five orders of magnitude. Due to the nature of discretization in FIMMWAVE, simulating a thick layer (in comparison to the wavelength) is not possible.

Table 2.6: Comparison of for the AGC-LD (1^{st} generation LDs, $\lambda_o = 435.5\,\text{nm}$).

Parameter	2-D, 3 µm substrate	1-D, 3 µm substrate	1-D, 300 µm substrate
n_{eff}	2.4691	2.4700	2.4698
α_{EV} (cm^{-1})	18.20	16.12	15.07
Γ_{QW}	2.29%	2.15%	1.98%
$\Gamma_{\text{substrate}}$	0.13%	2.9%	12.3%

In Table 2.6, the AGC-LD device described in §5.1 is simulated with both the 1-D TMM solver and the 2-D FIMMWAVE solver. However, the waveguide simulated in FIMMWAVE is restricted to a 3 µm-thick substrate, while the TMM solver can do both a 3 µm-thick and a 300 µm-thick substrate.

The values to note are the confinement factors of the QWs and the substrates. Due to the electric wall boundary at the bottom of the 2-D simulation, very little of the mode is present in the 3 µm-thick substrate. The 1-D simulation has real (aluminum) metal at the bottom, which allows for more mode penetration into the substrate. In the case of the 300 µm-thick substrate, a significant fraction of the power is present in the substrate and changes all of the laser's internal parameters as a consequence.

A simple rule can be followed to ensure that a mode is not leaking into the substrate: the simulated effective refractive index of the mode must be larger than the refractive index of the substrate. In the above case, the effective index of 2.4691 is less than that of GaN at 2.4863. Therefore, FIMMWAVE cannot be used to simulate the AGC-LDs (1^{st} generation LDs).

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Chapter 3

Low damage dry etch for GaN

Dry etching is the most common way to etch device geometries in GaN. Features that have been patterned lithographically are anisotropically transferred to the substrate using the biased plasma in a dry etch tool like a Reactive Ion Etch (RIE) or Inductively Coupled Plasma (ICP) machine. In contrast, there are no wet etching options to accurately transfer a lithographically defined pattern. Therefore, dry etching is the only option to etch nano-scale features like photonic crystals (PhCs) or the Etched Gap Cladding (EGC) described in **Ch. 2**.

Nano-scale features like PhCs or an EGC require close proximity to the optical mode of a waveguide in order to have a significant effect. Typically, the design requirements demand that the feature of interest be placed within two wavelength periods (e.g. $< 336\,\text{nm}$ for $\lambda_o = 450\,\text{nm}$ in GaN) of the light emitting active region. This means that the dry etched surface will be close enough that plasma damage may reach the active region and destroy device performance. [1] Though some etch damage to an active region can be partially recovered with high temperature ($\geq 500\,^{\circ}\text{C}$)

anneals, [2] avoiding etch damage altogether is preferred.

Special care must be taken to ensure that the active region maintains its light emitting capability throughout dry etching and the rest of the device fabrication. Prior to the fabrication of an InGaN/GaN laser diode (LD), we developed and tested a low damage dry etch to fabricate an EGC. In the experimental setup, the photoluminescence (PL) of an InGaN quantum well was carefully monitored for degradation as the sample was etched. The result was a compatible dry etch process and design rules for nano-scale features on the surface of LDs.

3.1 Dry etch damage in GaN

A common dry etch chemistry for GaN is a mixture of Cl_2 and Ar. The charge-neutral [Cl·] free radical is the most chemically active species used to remove Ga from the surface through the production of volatile $GaCl_x$. This process is assisted by bombardment of energetic ions in the plasma, namely [Ar^+] and [Cl^+].

The physical nature of ion bombardment aids both in breaking the [Ga]-[N] bonds as well as sputtering of the volatile species off the surface. [3, 4] The directionality of ions from the positively charged plasma to the negatively charged substrate allows for preferential etching that transfers the pattern anisotropically. The DC voltage bias is a direct measure of this electric field and a good way to gauge the force of ion bombardment.

3.1.1 Etch damage mechanisms

Plasma damage can happen through a variety of mechanisms and damage the semiconductor crystal below the etched surface. The ion bombardment can be mod-

elled in the same manner as ion implantation. [5] Thus, the concentration of crystal damage will extend into the substrate in a tear drop concentration profile and will depend both on the ion energy and crystal plane. However, even with a DC bias of $-200\,\mathrm{V}$, the simulated penetration of $[Cl^+]$ is only $\sim 2\,\mathrm{nm}$.

It is well known that sub-surface damage extends well beyond 2 nm. For instance, radiation-induced damage will penetrate deeper, perhaps up to 100 nm, and degrade InGaN QW emission. [5] In addition, it has been previously shown that planes with the largest open areas between lattice points will "channel" defects and allow for deeper penetration. [6] In this case, the **c**-direction will allow for the deepest penetration of sub-surface damage, followed by the **a**-direction and **m**-direction next (of the low-miller indices directions).

Dry etch both produces sub-surface defects and aids in their diffusion. [7] Therefore, the high concentration of surface and sub-surface defects produced by dry etch will diffuse away from the area of formation, spreading out while penetrating deeper into the substrate. There are a few energtic mechanisms by which this happens: (1) the ion bombardment transfers energy to the crystal lattice, raising the "local" temperature and increasing the diffusion constant; (2) visible and UV radiation produced by the plasma can be absorbed, increasing the diffusion constant; (3) any charged defect will feel a force exerted by the applied electric bias during the etch process and drift in accordance with electric field.

All damage-inducing and diffusion-enhancing mechanisms are related to the power input into the etch chamber. Of the two most common plasma power sources, inductively coupled plasma (ICP) power and capacitively coupled plasma (CCP) power, the CCP power is responsible for the bias voltage. It is this bias voltage that drives the anisotropic etching, as well as the first and third defect diffusion mechanisms. In

ICP dry etch machines, the plasma density and intensity is mostly controlled by the ICP power and will be the biggest factor in visible and UV radiation production.

3.1.2 Common GaN dry etch conditions

Using an ICP machine, we have a number of parameters to consider: total gas flow, gas ratio, chamber pressure, ICP power, and CCP power. On some machines, the cooling temperature can also be adjusted. While the specific gas flows and powers will be unique to each machine, typical CCP powers are around 100 W, with the resulting bias field around −200 V (DC) from the top electrode to the substrate. [3]

Processing parameters are adjusted according to need. Both DC bias and etch rate will increase greatly with CCP power, increase slightly with ICP power, but peak with gas flow, gas ratio and pressure. Side wall verticality will increase with CCP power and low ($\sim$ 1 mTorr) pressure. Etch damage will increase with DC bias (CCP power), slightly with ICP power and decreases slightly with pressure; it will also increase with radiation, which increases with total plasma power (ICP+CCP).

3.1.3 Low power plasma limit

The approach we take to lower etch damage is to lower CCP power as much as possible, and then to lower the ICP power as well. This should reduce both the penetration depth of sub-surface damage as well as minimizing the diffusion of defects. Since we will be using this etch for deep aspect ratio trenches that are only 150 nm-wide (EGC), we also use low pressure to facilitate transport (removal) of etch by-products. The resulting etch profile will tend to deviate from vertical side walls and is found to be very dependent on the total gas flow. A gas ratio of 50/50 was chosen simply to limit the variable space, knowing that it is adequate for proper dry

etch chemistry.

The etch rate will decline monotonically with decreasing CCP power, and will drop off sharply if too low. As found previously, this drop off occurs at around $-20\,\mathrm{V}$ of DC bias on the substrate. [8] It is important to consider that subsurface damage is directly proportional to the time under plasma. [7] Therefore, for a given etch depth, as the etch rate is decreased, the penetration depth of damage underneath the etched surface will increase. Minimizing the sub-surface etch damage will correspond to an optimal DC bias (given other parameters are similar).

After experimentation, it was found that even when fixing the DC bias just above the minimum of $-20\,\mathrm{V}$, an etch rate of $26\,\mathrm{nm/min}$ in c-plane GaN was achievable. However, at a DC bias of $-18\,\mathrm{V}$, there was no measurable etch depth or etch rate

3.2 Low power dry etch

GaN dry etching is performed in a Unaxis VLR high temperature ICP system. The chamber must be thoroughly cleaned and seasoned before a low power dry etch. This is because a low power plasma is much less stable and very sensitive to the chamber environment. Without chamber preparation, the plasma is difficult to maintain and the etch rate becomes sporadic. Special care must be taken to prevent chamber contamination and produce repeatable etch rates.

An alternative GaN dry etch was developed on a Panasonic E640 machine, but not investigated as thoroughly. Though final etch profiles and etch rates were moderately comparable, the large differences in chamber design prohibit direct comparison of processing parameters. In addition, the Panasonic machine uses an electrostatic chuck instead of a physical clamp which prevents measurement of the DC bias.

3.2.1 Choosing a carrier wafer

Particular care must be taken when choosing a carrier wafer. In the 4 in. Unaxis system, the common choices are either a Si or a sapphire carrier wafer, 1 mm thick. Considering that the inner lining of this system is entirely alumina, sapphire is a good choice for a carrier wafer since it will not change the chamber environment during etch. However, since it is an insulator, it will obscure the DC bias reading. In fact, the same etch recipe that has a DC bias of −20 V bias using a Si wafer registers −38 V with a sapphire wafer. Whether the increased DC bias is seen at the sample is not considered here.

Unfortunately, Si is particularly bad to use in a low power Cl_2/Ar etch. Si etches quickly in a Cl_2/Ar plasma and changes the chamber environment. This was evidenced by the fact that the slot valve used to maintain a constant chamber pressure started at 60

Deposited Ni metal is often used as a hard mask during chlorine-based dry etching, so its usefulness as a carrier wafer was explored. After dry etching using the recipe of interest for 15 min, 25 nm of electron-beam deposited Ni was removed. The nickel alloy Inconel 625 has even better corrosion resistance; after 15 min of etching, no noticeable etch depth could be measured. Therefore, wafers of Inconel 625 were machined to make carrier wafers for GaN pieces.

3.2.2 Etch preparations

The chamber is first cleaned for 5 min with a Cl_2/Ar etch and a sapphire cleaning wafer, then 1 h using O_2 plasma. The etch process is run using GaN dummy samples on a Ni-alloy carrier. The cleaning and chamber preparation removes contaminants

which have a profound impact on the plasma of the low-power Cl_2/Ar etch. It was observed that without this stable environment, the plasma would often go out or even fail to light during the ignition step.

The sample is mounted in the center of the Ni-alloy carrier wafer using Corning high temperature vacuum grease. The purpose of the grease is to maintain a repeatable and uniform temperature during etch. The sample is then closely packed with more GaN dummy samples in order to load the chamber.

Chamber loading improves uniformity across the sample. To test this, a 6 mm × 12 mm *c*-plane sample was etched with and without a 2 in. GaN wafer (Fig. 3.1.a). Without chamber loading, the sample varied in etch depth by ∼ 30% across 6 mm (Fig. 3.1.b), while a sample etched in a loaded chamber varied < 10%.

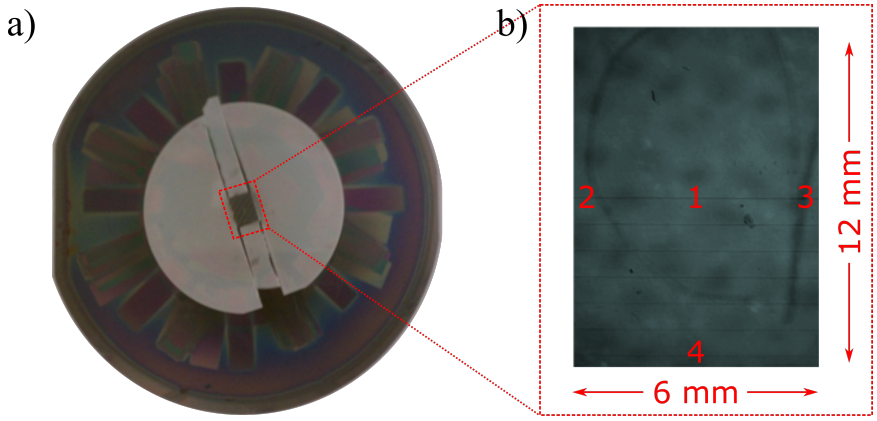

Figure 3.1: a) Etch sample mounted on a alumina-coated wafer surrounded by a 2 in. GaN-on-sapphire dummy wafer. **b)** Close-up of the *c*-plane etch sample, with the four etch depth measurement positions indicated.

3.2.3 In-situ surface clean

A native GaN oxide will delay the etch of GaN in Cl_2/Ar. Therefore, a pre-etch to remove GaO_x is used. Table 3.1 lists the process parameters for a Unaxis BCl_3 plasma etch of GaO_x. [9]

A 40 s etch is sufficient to remove the native oxide that grows on a GaN surface. It will etch ~ 10 nm at a DC bias of -154 V. It is only needed if the surface has not yet been disturbed. For instance, if an SiO_2 hard mask is used, the typical CF_4 etch used (with over-etch) to pattern the SiO_2 will suffice to remove GaO_x. If the GaN etch is performed immediately after (< 1 h), the pre-etch will not be needed. For the dry etch experiment described in §3.4, it is always used to maintain consistency.

After a few cycles of pumping and purging following the GaO_x etch, the GaN etch can be started without removing the sample from the chamber or breaking vacuum.

Table 3.1: *Top:* Processing parameters for GaO_x dry etch on the Unaxis VLR. *Bottom:* etch rates for various materials.

Parameter	Step 1: Stabilize Gas Flow	Step 2: Etch w/ BCl_3
Time (s)	40	40
Pressure (mTorr)	20	10
BCl_3 Flow (sccm)	10	10
He Pressure (mTorr)	5	5
RF 1 [*CCP*] (W)	0	40
RF 2 [*ICP*] (W)	0	500
RF 1 Tune/Load	38.5%/56.4%	*auto*
RF 2 Tune/Load	40.3%	*auto*

Material	Etch Rate (nm/ min)
SiN_x	6
Al_2O_3	28.2
c-plane GaN	12.3
m-plane GaN	15

3.2.4 GaN dry etch

The process steps for the low power GaN etch are listed below. The etch was thoroughly characterized with an assessment of the sub-surface etch damage (§3.4). During the etch, the carrier wafer is normally cooled to 200 °C (the standard setting of this tool) with backside He, though a single run at 50 °C did not seem to show a

difference in etch rate or sidewall profile.

Table 3.2: *Top:* Processing parameters for low power GaN dry etch on the Unaxis VLR. *Bottom:* etch rates for various materials.

Parameter	Step 1: Stablize Gas Flow	Step 2: Ignite Plasma	Step 3: Ramp Power	Step 4: Etch w/ Cl_2/Ar
Time (s)	40	5	5	*TBD*
Pressure (mTorr)	10	10	10	2
Cl_2 Flow (sccm)	10	10	10	10
Ar Flow (sccm)	10	10	10	10
He Pressure (mTorr)	5	5	5	5
RF 1 [*CCP*] (W)	0	10	5	5
RF 2 [*ICP*] (W)	0	500	200	200
RF 1 Tune/Load	40%	*auto*	*auto*	40/30
RF 2 Tune/Load	46%	*auto*	*auto*	40

Material	Etch Rate (nm/ min)
SiN_x	7.2
Al_2O_3	0
c-plane GaN	26
m-plane GaN	46

An alternative low power dry etch was also developed on the 6 in. ICP etcher, a Panasonic E640 (Table 3.3). The resulting etch profile of nanoscale features was characterized, but the sub-surface dry etch damage was not investigated.

Table 3.3: *Top:* Processing parameters for low power GaN dry etch on the Panasonic E640. *Bottom:* etch rates for various materials

Parameter	Step 1: Stabilize Gas Flow	Step 2: Ignite Plasma	Step 3: Ramp Power	Step 4: Etch w/ Cl_2/Ar
Time (s)	5/5/15/0	5/10/0/0	0/5/0/0	*TBD*/5/15/0
Pressure (Pa)	2	0.2	0.2	0.2
Cl_2 Flow (sccm)	22.5	22.5	22.5	22.5
Ar Flow (sccm)	22.5	22.5	22.5	22.5
He Pressure (mTorr)	700	700	700	700
Bias [*CCP*] (W)	0	0	0	30
Source [*ICP*] (W)	250	250	250	250

Material	Etch Rate (nm/ min)
SiO_2	12
m-plane GaN	63

3.3 PL test structure & test setup

The PL of a QW is very sensitive to etch damage. If we control for the various factors that affect PL, we can use it to determine whether a QW has been affected by etch damage or not. In contrast, QWs under electrical injection may not readily show evidence of etch damage, but the operational device lifetime of the final LED or LD may be significantly shortened.

Compared to electrical injection at typical LED or LD current densities, optically pumping QWs for PL emission results in a much lower carrier concentration. The

recombination rate (R) various types of carrier recombination are directly dependent on the carrier concentration, $[n]$, characterized by the "ABC model":

$$R_{total} = A[n] + B[n]^2 + C[n]^3 \tag{3.1}$$

where the A, B, and C terms are the trap-assisted non-radiative (NRR), radiative, and Auger recombination rates, respectively. We can now define the internal quantum efficiency as the ratio of the radiative recombination rate to the total recombination rate:

$$\eta_{\mathrm{IQE}} = \frac{B[n]^2}{A[n] + B[n]^2 + C[n]^3} \tag{3.2}$$

The NRR coeficient increases with etch damage. [10] Using experimentally fitted terms for A, B, and C, [11] we find that the NRR coefficient will be the dominate term in R_{total} for low carrier concentrations ($< 1 \times 10^{18}\,\mathrm{cm}^{-3}$). The radiative coefficienct is not expected to change with etch damage and the Auger term is more than an order of magnitude smaller than the other two recombination terms at low carrier densities, rendering small changes in C inconsequential. Therefore, any increase in the NRR coefficient will correspond to a significant (i.e. measurable) decrease in η_{IQE} when measured using a constant, low carrier concentration.

To see changes in NRR centers, we must control for all variables that affect PL. We can directly measure the change in PL before and after etch, which gives us the change in external quantum efficiency, η_{EQE}. The external quantum efficiency of the PL emission is given by:

$$\eta_{EQE} = \eta_{ext} \times \eta_{IQE} \times \eta_{in} \tag{3.3}$$

where η_{ext} and η_{in} are the extraction efficiency and light in-coupling efficiency, respectively. Experimental variance in light collection and differences in sample surface

roughness before and after etching will change both η_{ext} and η_{in}, obscuring any change in NRR centers.

Production and collection of PL must be carefully designed to avoid confounding factors that arise before and after dry etching. First, the etched sample must have approximately the same fermi levels and energy band diagram as un-etched, otherwise the QW carrier concentration and PL will change unexpectedly. Second, the change in light extraction from the device must be addressed — even a nominally smooth planar etch of an epitaxially smooth sample will show increased light in-coupling and extraction due to its unavoidable surface roughening. [12, 13] Finally the test structure and procedure should mitigate the problem of non-uniform light emission so that repeatable measurements can be taken.

3.3.1 PL test structure

To view etch damage vs. etch depth, we use a double-active region PL test structure adapted from prior work. [14] The first active region consists of a triple QW active region 550 nm below the surface. It is used as a single-point depth marker for etch damage. The second active region is again 3-QWs, another 550 nm below the first. It is assumed that this deeper set of QWs is deep enough to avoid etch damage during the first 700 nm of etching. To a first order approximation, changes in light extraction will scale equally for both active regions. Therefore, the deeper set of QWs is used as the normalization factor for the shallow set of QWs.

To easily separate the sources of light emission, the shallow and deep active regions emit at 469 nm and 417 nm, respectively. The *c*-plane (0001) orientation provides the narrowest full-width at half-maximum (FWHM) emission of the substrate options at UCSB. Optically pumping this *c*-plane sample with a HeCd laser emitting at 325 nm

allows for all three light sources to be discerned.

The *c*-plane of GaN should exhibit the worst amount of etch damage compared to the other crystal planes. As documented above, the Ga-face of GaN etches much slower than the *m*-plane. Combined with the largest channeling effect of any GaN plane, *c*-plane is the worst case scenario for dry etch damage.

The structure was grown on 2 in. double-side polished sapphire by metal organic chemical vapor deposition (courtesy of Dr. Nathan Young). The structure from top to bottom was as follows: 548 nm of n-type GaN, three pairs of 2.8 nm-thick unintentionally doped (UiD) $In_{0.2}Ga_{0.8}N$ QW with 7.1 nm-thick barriers, 548 nm of n-type GaN, another 3-QWs of $In_{0.11}Ga_{0.89}N$, and 8.5 µm of n-type GaN (Fig. 3.2). After growth, 165 nm of SiN_x was sputtered on top for later use as a dry etch hard mask.

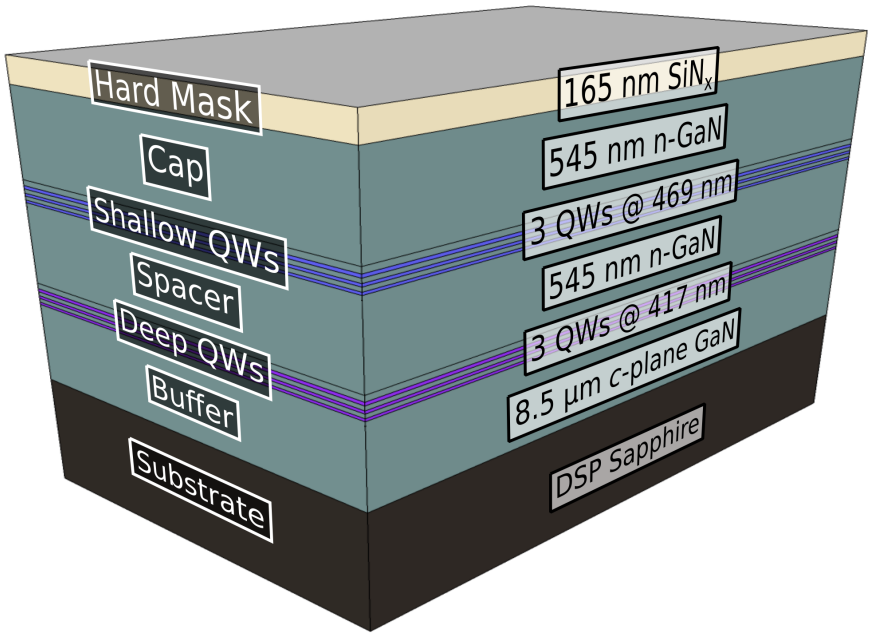

Figure 3.2: Schematic of a *c*-plane epitaxial growth with sputtered SiN_x on top and a double-side polished sapphire substrate.

The n-type doping was [Si] = $2 \times 10^{18}\,\mathrm{cm}^{-3}$, as measured by secondary ion mass spectrometry. It was chosen so that the predicted change in doping during dry etch would be minimal — p-type material would be heavily compensated, [15] leading to unwanted changes in carrier concentration. The thick buffer layer was necessary to reduce the Fabry-Perot fringing that arises from the cavity of the GaN surface and the substrate.

The wafer was cleaved into 6 mm × 12 mm samples (Fig. 3.1.b), of which the seven with the brightest PL were selected. The samples were then lithographically patterned with mesa stripes ranging from 2.5 µm to 10 µm wide. These stripes are used to measure the etch depth via atomic force microscopy (AFM). These mesa stripes will remain un-etched, but cover $< 5\%$ of the total surface area. Prior to the GaN etch, the SiN_x was etched by ICP using a CHF_3/CF_4 etch chemistry in which GaN does not etch.

3.3.2 PL test setup

The choice of PL setup is greatly dependent on the sample. A typical PL setup will have a spot size of 1 mm^2. For the above sample, slight growth variation together with a Fabry-Perot fringe spacing of ~ 11 nm resulted in a highly peaked and position-dependent PL measurement that was un-repeatable. The same growth on a bulk GaN substrate may have been more successful, but significantly more expensive.

Instead, a Perkin Elmer LS 55 Fluorescence Spectrometer was used to measure PL spectra. With a spot size of 75 mm^2, the spatially-dependent Fabry-Perot fringing is averaged out to produce a smooth PL spectrum (Fig. 3.3).

The white-light pump source is filtered via diffraction grating to 385 nm. The high intensity pump will excite carriers in the QWs without producing carriers in

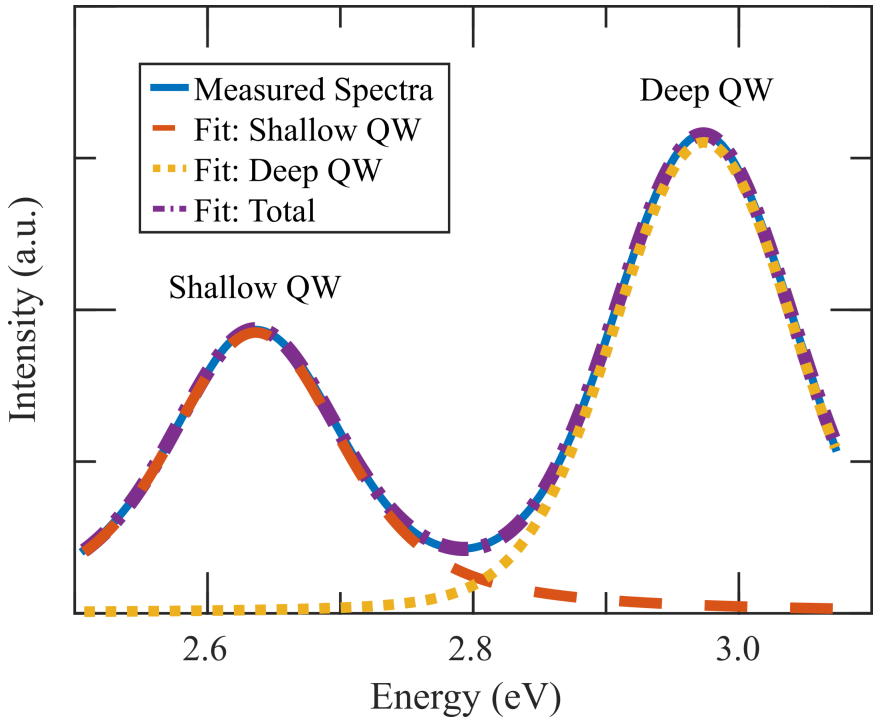

Figure 3.3: Typical PL data of a double-active region sample. Each PL peak is fit with a Voigt function in the energy domain.

the surrounding GaN. The pump source is further filtered using a 11 nm-bandwidth external filter centered at 386 nm to clearly resolve the PL spectra.

With this structure and setup, the PL spectra can be resolved clearly and repeatably. The Voigt function, a convolution of Gaussian and Lorentzian lineshapes, proves to be an excellent fit for the PL emission. To evaluate the repeatability, the same test sample was measured 13 times, breaking down and reassembling the test setup each time. The integrated intensity of the PL fits had a standard deviation of 13% and 10% for the shallow and deep QWs, respectively. When the intensity of the deep QWs was used as a normalization factor, the standard deviation was only 5%, showing that the double-active region technique functions to reduce the experimental error of the test setup.

3.4 PL vs. etch depth

After growth and SiN_x deposition, the seven cleaved samples underwent the following procedure:

1. The samples were lithographically patterned and the SiN_x hard mask was etched in CHF_3/CF_4 chemistry
2. PL spectra taken using Perkin Elmer LS 55 Fluorescence spectrometer with a 10 nm-bandwidth, 385 nm external filter
3. The seven samples subjected to 2 min (24.6 nm) of in-situ surface clean to remove GaO_x
4. Six of the samples underwent the low-power Cl_2/Ar dry etch for various times, up to 1300 s
5. The post-etch PL spectra of all samples was taken
6. The SiN_x hard mask was removed in HF
7. The etch depth of the seven samples was measured by AFM in four positions (Fig. 3.1.b)
8. High-angle dark field scanning transmission electron microscopy (HAADF-STEM) was done on one deeply etched sample for etch surface-to-QW distance measurements

Careful measurements of the PL, etch depth, and QW depth are taken in order to view the change in PL versus the etched surface-to-QW distance.

3.4.1 Etch depth measurement

The seven samples were etched between 0 s (in-situ surface clean only) and 1300 s. From AFM measurement, the in-situ surface clean and low-power etch rates were determined to be 12.3 nm/min and 26 nm/min, respectively. The range in etch depth measurement between the 4 measurement points was ~ 2 nm.

AFM was also used to inspect the etched GaN surface. After the in-situ clean, the root mean square surface roughness, σ_{rms}, of a 5 µm × 5 µm area was 0.55 nm. This roughness increased linearly at a rate of 0.13 nm per 100 nm etched. More importantly, it was found that numerous pits formed and were preferentially etched at a different linear rate than the surface, extending below the nominal etched surface at a rate of 10 nm per 100 nm etched (Fig. 3.4).

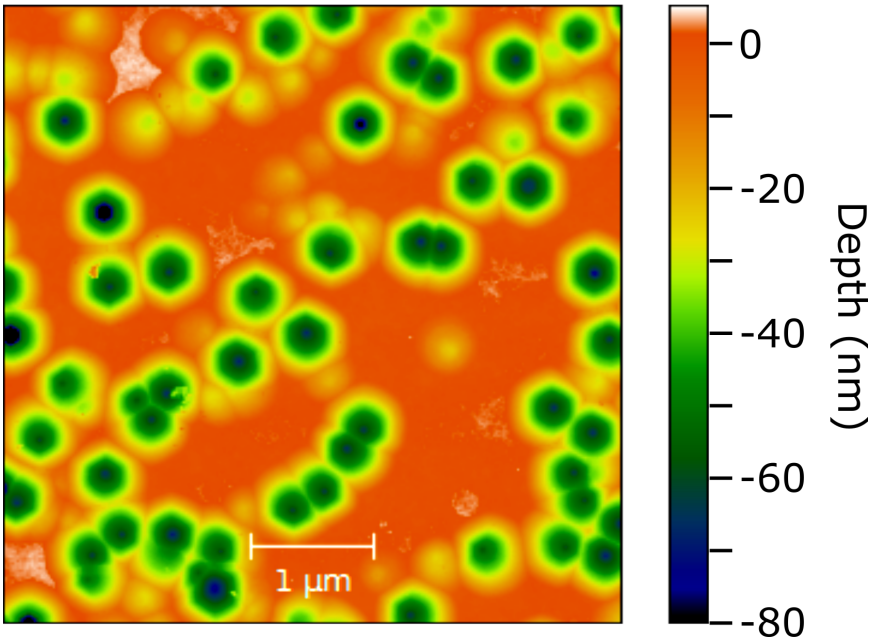

Figure 3.4: AFM image of the etched GaN surface (@ 0 nm), 607 nm below the un-etched surface. Preferentially etched hexagonal pits extend $\sim$ 60 nm below and cover $^2/_3$ of the surface.

The hexagonal pits are in the correct order of magnitude to be attributed to threading dislocations at $3 \times 10^8\,\mathrm{cm}^{-2}$ [16] and have been observed previously observed after etching. [4, 17] These pits are expected to greatly increase the extraction efficiency and would confound accurate PL measurement without a normalization factor. However, since these pits decorate threading dislocations, these pits are not observed on low dislocation ($5 \times 10^6\,\mathrm{cm}^{-2}$, [18]) bulk GaN m-plane substrates.

The etch depth measurements were converted to distances away from the shallow QW by measuring HAADF-STEM micrographs (courtesy of Dr. Yanling Hu). Fig. 3.5 shows the etch profile of a GaN stripe measured to be 530 nm by AFM. The etched surface is 24.6 nm away from the top of the first QW. With the distance to the shallow QW calibrated, a precise PL vs. etch depth can be constructed.

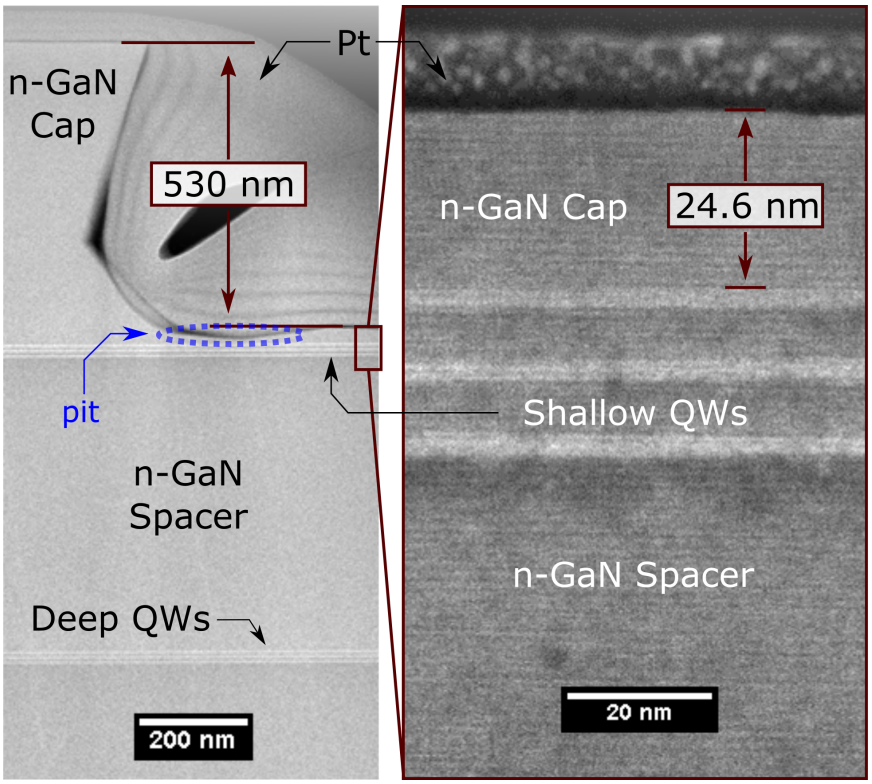

Figure 3.5: Cross-section HAADF-STEM images of the *c*-plane on sapphire double-active region test structure. The sample has been etched 530 nm and shows a deeper etched pit next to the un-etched mesa. Platinum is deposited on top as part of the STEM procedure.

3.4.2 Normalized PL measurement

The relative [post-etch PL] vs. [pre-etch PL] measurements are compared to give a picture of proportional changes in η_{EQE}. The integrated intensity ratio of the deep QWs steadily increased with etch depth to 150% of its original after 500 nm of etching. This is a clear indication that the in-coupling and extraction efficiency have increased. It is primarily due to the increased surface roughening and pitting of the etched surface.

The integrated intensity ratio of the shallow QWs also increased with etch depth

until it dropped off suddenly. This drop-off is due to the decrease in η_{IQE}, a direct consequence of etch damage. Using the integrated intensity ratio of the deep QWs as a normalization factor, we can now view the effect of etch damage on the PL as the etched surface approaches a light emitting QW (Fig. 3.6).

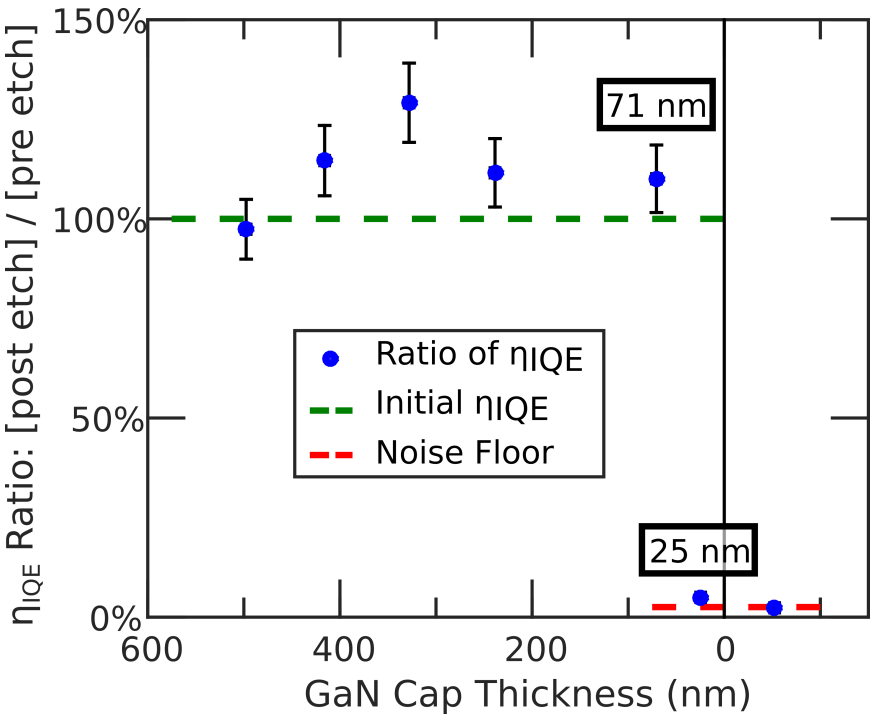

Figure 3.6: Percentage change of η_{IQE} as a low-power dry etch approaches QWs through a GaN cap. No deterioration of η_{IQE} is observed down to a measured thickness of 71 nm.

The experiment shows that light emission stays nearly constant up to 71 nm away (corresponding to a 484 nm etch depth), after which severe deterioration occurs. This value is extremely conservative: besides occurring on *c*-plane which has the slowest etch rate and is most affected by channeling of etch damage, the substantial surface pitting extending 10% further after 484 nm of etching brings much of the etched surface closer to QW.

For the data point of interest, the average distance from the QWs is actually 53 nm away, with the deepest part of the pits approaching 25 nm. Therefore, this etch may allow for a planar etched surface to come to 50 nm away from a QW without the QW experiencing deterioration of the light emission. At the next data point of 25 nm away, many of the pits have already penetrated the QWs, removing much of the active region altogether.

3.4.3 Design rules for surface etched features

We can now use the following design rules with the documented dry etch: on high dislocation density substrates, e.g. *c*-plane on sapphire, an etched surface can approach 50 nm away from a light emitting active region as long as the etched pits do not exceed 25 nm deep. This limiting scenario would be a 250 nm-deep etch. On low dislocation density substrates, e.g. bulk GaN, a planar etched surface can approach a QW up to 50 nm, regardless of the etch depth.

This design rule is easily satisfied with the EGC LD designs demonstrated in **Ch. 2**. Therefore, this dry etch is a useful fabrication process for EGC LDs and other nanoscale optical features.

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Chapter 4

Process steps for EGC-LDs

The surface-etched nano-structures that constitute the top cladding layer require a number of specialized processing steps compared to a standard ridge laser design. Aside from the developed low-damage dry etch, non-standard lithography techniques and dielectric layers are required to fabricate an etched-gap cladding (EGC).

Patterned features smaller than 0.5 µm require lithography beyond the standard i-line (365 nm light source) lithography systems. In this work, we utilize two different methods to achieve 300 nm-pitch stripes: holography (at 325 nm) and electron beam lithography. Two more methods for patterning small features are available at the UCSB nanofabrication facility: nano-imprint lithography and deep UV (248 nm).

For a process compatible dielectric to fill the EGC, we utilize the spin-on dielecric benzocyclobutene (BCB) in the 2nd generation LD devices. Its advantages include a natural planarization effect and chemical resistance to HF acid. Because it does not etch in HF, we can use an SiO_2 layer as an etch hard mask and easily remove the SiO_2 afterwards.

The step-by-step processing followers can be found in *Appx. D.* §D.1 is the follower for the holography process used to fabricate the first device demonstration, an air-gap cladding laser diode (AGC-LD). §D.2 is the full process for the second device demonstration, the etched-gap cladding laser diode (EGC-LD).

4.1 Holography on GaN

The holography system at the UCSB Nanofabrication Facility is a Lloyd's mirror interference lithography system. The light source is a 325 nm HeCd laser that is collimated and expanded to produce a coherent, uniform intensity beam over a $4\,\mathrm{cm}^2$ area. The stage for mounting the sample also holds the mirror, fixed at 90° to the sample. A $2\,\mathrm{cm} \times 2\,\mathrm{cm}$ sample can be exposed to create a grating aiming the beam at the intersection of the sample and mirror, so that the coherent light will constructively and destructively interfere with its angled reflection.

The pitch of the grating pattern is determined by the wavelength of the laser and the angle of the stage & mirror with respect to the beam. The wavelength of the HeCd laser is very stable. A pitch of 200 nm - 300 nm can be obtained repeatably by setting the stage angle, according to:

$$\theta_{stage} = 2\sin^{-1}\left(\frac{\lambda_o}{2\Lambda}\right) \tag{4.1}$$

where λ_o is the light source wavelength (325 nm) and Λ is the desired pitch. The stage angle is aligned to the normal of the mirror, so that the incident angle on the sample is:

$$\theta_{incident} = 90° - \theta_{stage} \tag{4.2}$$

The fill factor of the pattern is determined by the photoresist (PR) used and the exposure energy. The output power of the laser will drift with time. It was found

to be most stable for a 1 h window after a 1 h warm-up period. After measuring the output power, the exposure time is calculated from the required exposure energy. Even with careful calibration, a 50% fill factor pattern was found to vary by ±10 percentage points. An LD design featuring an EGC is generally very tolerant to such variation. However, the dry etch for the EGC will change depending on the fill factor, making the processing much more difficult.

Fig. 4.1 shows the progression of holography development, detailed in §4.1.1 and §4.1.2.

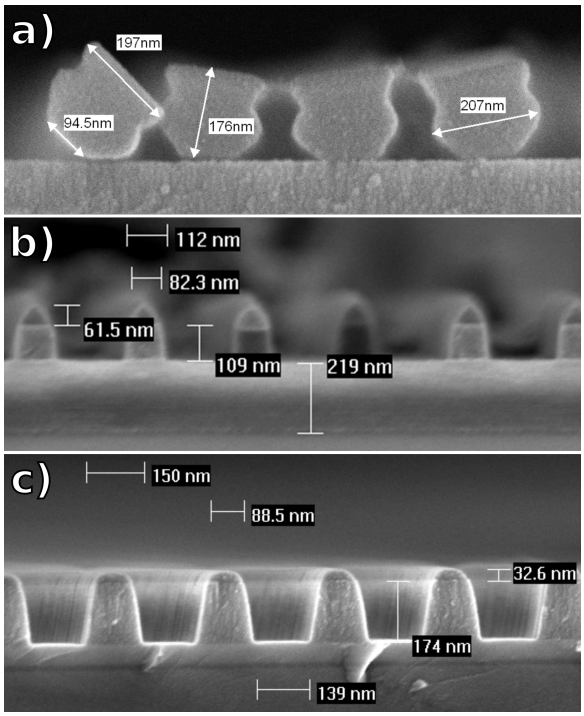

Figure 4.1: Cross-sectional SEM of developed holography PR on an ARC layer: **a)** positive-tone PR + un-calibrated spin-on ARC thickness, un-etched; **b)** positive-tone PR + calibrated spin-on ARC thickness, un-etched; **c)** negative-tone PR + calibrated SiN_x ARC thickness, etched

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4.1.1 The anti-reflection coating

The PR for interference lithography is very sensitive to standing waves within the resist. An anti-reflection coating (ARC) must be used, otherwise width of resist features will vary vertically, even to the point of pinching off and causing the resist to topple. One option is to use a spin-on ARC between the GaN and PR. The ARC heavily absorbs the light the passes through the resist. Additionally, the thickness is chosen to minimize reflection, which requires some modeling and/or calibration. Fig. 4.1.a shows the result of an improper ARC thickness on a holography pattern.

A spin-on ARC works well to reduce standing wave reflections, but must be patterned itself. With small features, developable ARCs tend to undercut too much, causing the resist to topple once again. Therefore, an "ashable" ARC is typically used. These ARCs require an O_2 plasma etch to transfer the resist pattern into the ARC.

The O_2 plasma will etch the resist as well, rounding the top and reducing the amount of resist available to etch the GaN (Fig. 4.1.b). Since interference lithography resist must be thin ($< 300\,\text{nm}$), maintaining a tall PR profile for dry etch can be critical.

Instead, we make the ARC using a layer of deposited SiN_x. The refractive index of the ARC layer should be close to the geometric mean of the PR (~ 1.7) and GaN (~ 2.57), around $n = 2.1$. The refractive index of stoichiometric Si_3N_4 is close at $n = 2.13$. The layer should also have the correct thickness given approximately by:

$$d_{\text{SiN}_x} = \frac{m\lambda_o}{4\ n_{\text{SiN}_x}} \cos\left(\theta_{\text{SiN}_x}\right), \quad m = 1, 3, 5... \tag{4.3}$$

where the angle in SiN_x is derived from Snell's law:

$$\theta_{\text{SiN}_x} = \sin^{-1}\left[\frac{\sin\left(\theta_{incident}\right)}{n_{\text{SiN}_x}}\right] \tag{4.4}$$

Choosing $m = 5$ results in a SiN_x thickness of approximately 175 nm for a 300 nm-pitch grating. The SiN_x can now serve as a hard mask for up to 600 nm of GaN low-damage dry etch in addition to serving as the ARC during holography.

4.1.2 Positive tone vs. negative tone photoresist

The holography fabrication was performed with two photoresists, one positive tone (THMR-IP3600HP-D) and one negative tone (TSMR-iN027), both from Tokyo Ohka Kogyo Co., LTD. The positive resist is usually spun on a little thicker at $\sim$ 285 nm, while the negative resist is $\sim$ 175 nm. To get a 50% fill factor, the negative PR requires more exposure energy at 120 mJ compared to 75 mJ for the positive PR. However, the resulting pattern is at the lower exposure limit for the positive PR.

In general, the positive PR is better for producing $<$ 50% fill factor patterns, while the negative PR is for fill factors $\geq$ 50%. Otherwise, the pattern will suffer from severe line edge roughness, to the point of bridging between the individual PR stripes. Since we intend to have a $\geq$ 50% fill factor, negative PR was ultimately chosen.

Though easier to pattern the intended fill factor, the negative PR is thinner than the positive PR, limiting the etch depth that can be achieved in the hard mask. Fig. 4.1.c shows the result of a SiN_x hard mask etch. After etching the 174 nm of SiN_x, only 33 nm of negative resist remains, and the sidewalls are clearly rounded.

In Fig. 4.1.c, the SiN_x hard mask is acting as a $^5/_4$ λ anti-reflection coating. The other two options are $^3/_4$ λ ARC (104.4 nm) and $^1/_4$ λ ARC (34.8 nm). The current layer is capable of masking the GaN beneath it during a dry etch of $\leq$ 800 nm. For $\leq$ 480 nm or $\leq$ 160 nm, the smaller two thicknesses would work much better and produce features without any rounding.

Negative PR can be patterned a second time to prevent etching in certain areas. Therefore, an i-line stepper process can be applied to the same PR in order to localize the etch-gap pattern. If instead a lift-off process was used to create a hard mask, positive PR would serve the same role. Such processes were briefly considered, but not fully developed in this work.

4.2 Electron beam lithography on GaN

Electron beam lithography is useful for patterning precise and complicated nano-structures. It is more expensive and time consuming than most lithography options, but remains an invaluable research tool.

We develop an e-beam lithography process on GaN that produces precise and repeatable EGC structures while minimizing line-edge roughness and tool time. In doing so, we realize a new fabrication method to create a lift-off mask on materials (GaN or otherwise) that have large electron backscatter.

4.2.1 Negative-tone bi-layer resist process

The EGC-LD device demonstration builds upon prior work [1] to create a lift-off mask for metal. The bi-layer resist consists of a top layer of hydrogen silsesquioxane (HSQ) and an under-layer of poly methyl methacrylate (PMMA). The HSQ is a negative-tone electron-sensitive resist that requires high exposure dosages compared to PMMA, but produces high resolution patterns after development in a 25% TMAH solution. In addition, a thin (10 nm) layer of aluminum deposited on top serves as a conductive path to ground for trapped electrons, but is easily removed after 10 s of development. In this usage, the PMMA does not play its normal role of a postive-tone

resist, but is simply an under-layer to assist in metal lift-off.

HSQ is a unique electron beam resist in that it forms a psuedo-SiO_2 layer when exposed. This renders the exposed HSQ inert in an O_2 plasma. Therefore, after exposure and development, the HSQ can function as an O_2 etch mask for an under-layer. With high selectivity, the under-layer can be much thicker than normally achievable with e-beam lithography. With only a 30 nm layer of HSQ, a 90 nm under-layer of PMMA can be patterned, with an undercut, for the purpose of Ni lift-off. In this case, we lift of 30 nm - 40 nm of Ni (deposited afterwards by electron-beam deposition).

The under-layer thickness is limited by the pattern dimensions. If the pattern is too thin compared to the layer thickness, the undercut during O_2 etch will undercut the pattern, causing it to fall over. This can be mitigated by using a directional etching system, like reactive ion etching. However, the O_2 plasma will inherently roughen the patterned HSQ. Therefore, one should choose an under-layer that etches quickly in O_2 plasma.

There is a lot of freedom when choosing an under-layer. The requirements are that it spins on to the desired thickness, is easily etched in O_2 plasma, and is compatible with e-beam lithography and HSQ. Many photoresists and polymers may suffice, but PMMA is easy to work with and well developed. One caveat that was discovered with PMMA is that the high dosage required by HSQ will shrink the PMMA by 50%. This did not affect the final process for the EGC-LD, but may need to be considered in other cases.

4.2.2 Edge-biased exposure technique

The e-beam lithography pattern is heavily influenced by the backscatter of electrons off the semiconductor. This acts as another dosage source, but unlike the sharply defined beam, it is closer to Gaussian random noise. This noise adds a background energy level to the original beam. The relative integrated backscatter energy is a function of the material, while the range and distribution is a function of the incident energy. The backscatter will reduce the required incident dosage, but increase the signal-to-noise ratio (leading to increased line edge roughness — LER). It is therefore very important to determine the amount of relative backscatter energy at a locations surrounding the beam, then adjust the dosage in that area accordingly. [2, 3]

The backscatter cross-section is determined by the material it is impinging on, and generally increases with increasing atom size. For instance, GaN and GaAs substrates will backscatter much more than Si substrates, simply due to the fact that the Ga atom is much larger than Si. [3] Therefore, the dosage required to expose resist on GaN compared to resist on Si will be less, but the signal to noise ratio will be higher. Exposure calibrations on Si and GaN showed clear evidence of this — using the same dosage scheme and pattern, 150 nm-wide lines on Si had LER of $\sigma_{\text{rms}} < 1\,\text{nm}$ while on GaN the LER was $\sigma_{\text{rms}} = 4\,\text{nm}$.

The amount of backscatter at a location due to fixed beam shot depends on the dosage within an area of influence. From Monte Carlo simulations [4] of 100 keV electrons impinging on GaN, this area of influence is approximately 158 nm in radius. Therefore, reducing the overall dosage in the proximity will reduce the backscatter. Care must be taken not to underexpose the pattern. Using the commercial software Beamer, [5] we can input the Monte Carlo simulation and our intended pattern to develop a dosage variation of the base dose. In general, this means the edges and corners

of patterns require higher dosage than the centers, due to the reduced backscatter in the proximity. We now apply this proximity area correction (PEC) to the base dose of all patterns.

The end result of PEC is that the intended pattern is nearly uniformly dosed. However, it does not address the LER of the pattern. If backscattered electrons is a source of noise at a specific location, then reducing the backscattered electrons will reduce the LER. Therefore, regarding only the line edge, as long as the edge of the pattern is not underexposed, reducing the total exposure dosage of a pattern in the area of influence will reduce the LER.

Assuming our goal is to use the resist layer as a lift-off mask, we can now develop a method for reducing the overall dosage. Using negative-tone resist, we can reduce the exposure in the middle of a patterned geometric shape to the point just above where the resist clears. Since the resist is only being used for lift-off, it does not matter if the full thickness is exposed. The only requirement is that a "shell" of resist remains to be lifted-off.

Reducing the dosage in the middle of a geometric shape will cause the line edge to be under exposed. To compensate, the exposure dosage on the edge must be increased. As long as the total increase in edge exposure is less than the total decrease in center exposure within any area of influence, the total backscattered electrons will decrease, along with the LER. Therefore, the dose calibration procedure for the edge-baised exposure technique is as follows:

1. Run a Monte Carlo simulation of the electron beam energy impinging on the material stack (substrate, deposited materials, resist) to get a relative backscatter distribution.

2. Use the backscatter distribution to perform PEC on your intended pattern.

3. Perform electron beam lithography dose calibrations to find the dosage that best recreates the original pattern. Use the smallest step size possible at this dosage.

4. Break the pattern into "center" and "edge" patterns, where the "edge" pattern consists of a one-step size-wide perimeter of each LER-critical shape.

5. Reduce the dosage of the center pattern until just before the center of the shape begins to clear; maintain the same edge pattern dosage. If necessary, increase the step size of the center pattern.

6. Increase the edge pattern dosage until the shape edges reappear. If possible, decrease the step size of the edge pattern.

7. If necessary, shrink the pattern by pulling the edge pattern inward so that the intended geometry is reproduced; shrink the center pattern by the same amount.

8. Repeat steps 5-7 until the center pattern dosage cannot be reduced further.

Fig. 4.2 illustrates the exposure scheme of a 150 nm-wide line of negative resist for lift-off. The equivalent area base dosages of the red, green, and blue shot patterns are 40 $\mathrm{mC/cm^2}$, 300 $\mu\mathrm{C/cm^2}$, and 600 $\mu\mathrm{C/cm^2}$, respectively. Compared to the normal, uniform dosage of 1 $\mathrm{mC/cm^2}$, the total dosage has been reduced by 49%.

The edges of the 150 nm-wide stripe are defined using a very high dosage. It is written in a single line of the smallest step size allowed by the tool. A number of passes are used to average out statistical noise in shot placement. Combined with the macroscopic reduction in dosage, the collective effect reduces the LER from $\sigma_{\mathrm{rms}} =$ 4 nm to 1.4 nm.

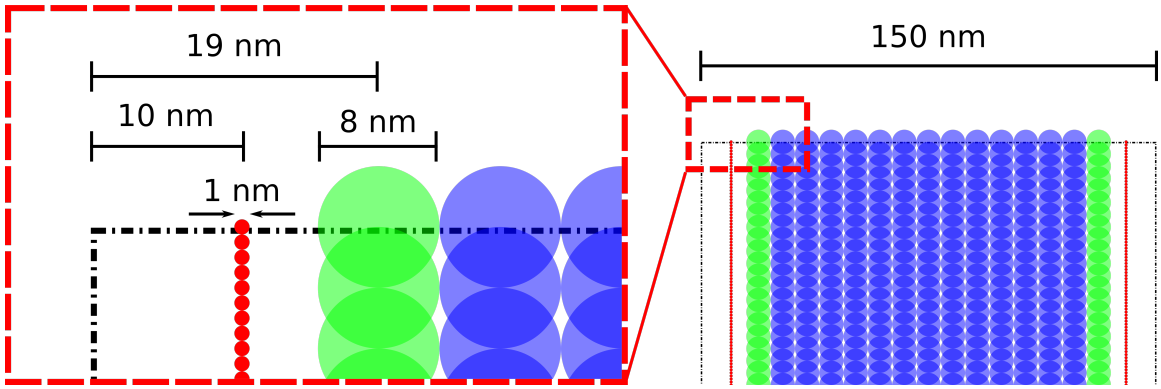

Figure 4.2: E-beam exposure placement and dosage across a 150 nm-wide line (*right*), with a zoom-in of one corner (*left*). The red circles are 1 nm-step shots of base dose = 0.1 nC per shot; it is repeated four times. The green circles are 8 nm-step shots of base dose = 0.096 nC per shot, repeated a second time with a 4 nm vertical shift. The blue circles are the same as the green circles, but at twice the dosage.

After metal lift-off, the LER increases to $\sigma_{\text{rms}} = 2\,\text{nm}$. The LER of the edge-biased resist is still a large contributor to LER, but it has been reduced by a factor of 3. This optimized thin metal pattern can then be transferred into a much thicker SiO_2 layer (Fig. 4.3) via dry etch.

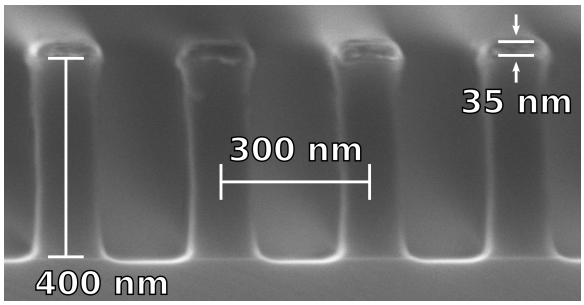

Figure 4.3: SEM cross-section of a thin Ni and thick SiO_2 hard mask patterned by electron beam lithography and dry etch.

An added benefit of the edge-biased exposure scheme is that the total exposure time is reduced. A 1-to-1 correlation of dosage and tool time means that the total

write time is cut in half. As an example, the EGC-LD device demonstration took 3.5 h to write instead of 6 h. Long write times on an e-beam lithography tool are expensive, in addition to slowing throughput; using an edge-biased exposure scheme saves on time and cost.

4.3 Other lithography options

The remaining lithography options available at the UCSB Nanofabrication Faciltiy are considered for the purposes of future process development.

4.3.1 Nano-imprint lithography

Nano-imprint lithography on GaN has been previously explored by Dr. Jason Jewell. [6] His process begins with a separate lithography technique (e.g. holography) on a Si substrate, which is subsequently dry-etched to produce a 2-D pattern of pillars. The patterned Si is then used as mask or "stamp" to pattern resist on GaN. The resulting pattern on GaN is the corresponding pattern of 2-D holes. The benefit of this method is that the same Si mask can be used a number of times before it gets worn out, after which a new patterned mask is made. However, it was found that while the process to produce holes was repeatable, other patterns like pillars and 1-D stripes of PR would often topple over.

4.3.2 Deep UV lithography

Deep UV lithography has a comparable minimum feature size of 120 nm, but these features can be intricate and non-repeating. It is advanced projection lithography system that requires very flat and well-aligned samples, with a minimum wafer diameter

of 100 mm (for the system at the UCSB Nanofabrication Facility). Unfortunately, the work done here is on much smaller pieces, disallowing the use of the DUV lithography system. Otherwise, DUV lithography would be the preferred method of lithography for etched-gap cladding and similarly sized features on GaN.

4.4 Etched-gap cladding fill material

The effective refractive index of the etched-gap cladding layer can be tuned by both the fill factor and the material used to fill the etched trenches. Many non-absorbing dielectric options will produce a sufficient index contrast when using a 50% fill factor. The larger concern is the process compatibility of the dielectric.

The deposition method of the dielectric must be able to uniformly fill the deep aspect ratio trenches. A directional deposition method like electron beam deposition and sputter will be susceptible to shadowing effects that will cause voids within the trench. Conformal deposition methods like atomic layer deposition and plasma enhanced chemical vapor deposition will leave "keyhole" voids as the trench is filled and pinches off. However, this keyhole can be minimized with certain trench sidewall geometries. If the trench geometry is repeatable, the keyhole void will be as well. The final method is spin-on of dielectrics. Any spin-on material is well suited to filling voids, but may come with other processing challenges.

After deposition, the dielectric must withstand further processing. This includes formation of a ridge and deposition of the p-contact metal. The dielectric must also be removed from the top GaN surface to allow for the metal contact. Therefore, the cladding fill process is a planarization process; planarization is, in general, a difficult fabrication problem.

4.4.1 Air-gap cladding

An often overlooked dielectric choice is air, making the cladding layer an air-gap cladding (AGC). Leaving air voids means that the gaps must be sealed in some manner. Previous work has used regrowth to coalesce the etched gaps. [7] The regrowth was also necessary for etch damage recovery as well. In general, regrowth is a difficult and expensive step, and puts large constraints on the fabrication process. Without the need for etch damage recovery, we can avoid regrowth. Instead, we use an angled-deposition of metal for the first generation of AGC-LDs.

If a sample is angled within a directional deposition system, any high aspect ratio features will be shadowed. In an electron beam deposition system, the sample is angled with respect to the source to take advantage of the shadowing effect. Fig. 4.4 shows the result of Pd deposition after an angled deposition of 60° from normal.

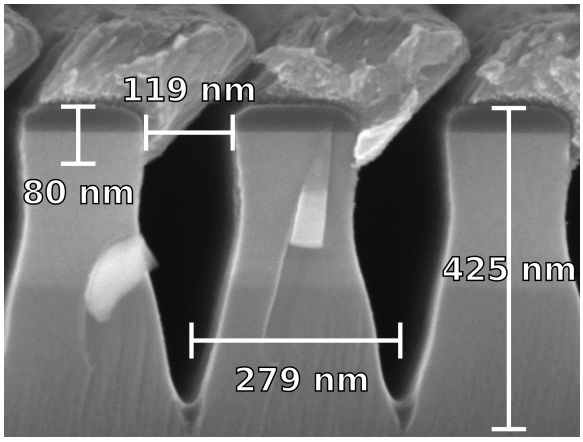

Figure 4.4: SEM cross-section of angled (60°) Pd deposition on a GaN and SiN_x air-gap test structure.

The AGC is capped by the Pd with 80 nm penetration into the air gaps. To avoid optical absorption by metal, the AGC must be thick enough to isolate the mode from the metal. Therefore, this technique prohibits the use of a thin ($\leq$ 150 nm) AGC

layer.

The Pd contact is followed by an Au pad deposition. The Pd does not coalesce immediately, so the following deposition of Au must be done at 0° from normal to electrically connect the contact area.

Structurally, air gaps capped by metal are lacking compared to standard device designs, e.g. a shallow ridge LD structure. By not contacting the entire surface area, the deposited metal is susceptible to delamination. In addition, the air gaps can unintentionally be filled with another material. This could be other liquids during fabrication (e.g. solvents, acids) which would exacerbate delamination. The air gaps could also be filled with the capping metal itself, either by physical forces or via electro-migration of metal during operation. However, angled metal deposition is a quick solution to the planarization issue of surface-etched nano-structures.

4.4.2 Spin-on benzocyclobutene

BCB is a polymer that can be spun-on and re-flowed (baked) for the purpose of planarization. It is electrically insulating and optically transparent in the visible spectrum. At 450 nm, the refractive index is 1.54.

The material properties of BCB make it a good candidate for a dielectric fill material, with the exception of its adhesion to other materials. Metals easily delaminate from BCB and other dielectrics require a very clean surface to adhere to BCB. For this reason, the recommended procedure is to use a thin (10 nm) sputtered layer of SiN_x with an in-situ back-sputter clean as an adhesion layer for metals. In contrast, BCB sticks extremely well to GaN. In a simple test, a stack of BCB, SiN_x, Ti, and Au were deposited on GaN and tested for adhesion using tacky Kapton® tape. The adhesion strength of the tape is well beyond the device and processing requirements,

yet none of the stack delaminated, demonstrating that the delamination issues of BCB can be completely avoided.

BCB is resistant to most acids and bases. For instance, it is unaffected by HF, allowing for wet etching of other common dielectrics like SiO_2. It can be removed by a combination of acid and oxidizing agent like a piranha etch, or dry etched with CF_4/O_2 plasma. Therefore, patterning BCB can be done in two ways: either by using the photo-sensitive variant and directly patterning it, or patterning with a traditional PR mask and dry etching.

Planarizing with BCB often requires spinning on a very specific thickness. The choice of thickness falls broadly into two approaches. First, a thick (many microns) layer can be deposited, then carefully etched back to reveal the top surfaces of the sample underneath. For instance, in the case of a 1 µm-tall, 10 µm-wide ridge, 4 µm of BCB were needed to reduce the height variation to < 100 nm. This method works well to planarize the entire chip area, but requires careful dry etching to remove the majority of the BCB. The second method is to spin a thin layer (< 500 nm) that only planarizes nano-structures. Etched gaps 150 nm wide will be completely filled and planarized to < 20 nm height variation, but the above ridge will not be planarized at all. However, the BCB will coat the sidewalls with the same thickness near the top of a microscopic feature, expanding in a sloped fashion to the lower etched surface.

In our second fabricated device, we used a 300 nm layer of BCB fill the etched gaps. To deposit this thin layer, non-photosensitive BCB (BCB-3022) was diluted with two parts Anisole and spun on at 4 krpm. After deposition and baking at 250 °C, the BCB thoroughly filled in the etched gaps in the GaN and left a nominal 300 nm at the top of the GaN surface (Fig. 5.9—*top*).

The BCB also served as the field dielectric, separating the p-metal from the semi-

conductor. However, it was found that the PR stripper 1165 causes BCB to swell, forcing pockets of delamination from the GaN surface. In Fig. 5.9 (*left, right*), the delamination of BCB from the GaN ridge sidewall can be seen. Therefore, using BCB requires using alternative solvents during further processing, like Acetone, which are not absorbed by BCB.

4.4.3 Other dielectric options

Conformal deposition of Al_2O_3 was briefly investigated as an EGC fill material. ALD was chosen for its conformal deposition properties to achieve repeatable fill in of trenches. However, filling in a 150 nm-wide trench requires a 75 nm deposition, which is beyond the recommended 50 nm limit for the machine used. Regardless, a long ALD deposition can achieve a clean and extremely conformal fill in of trenches.

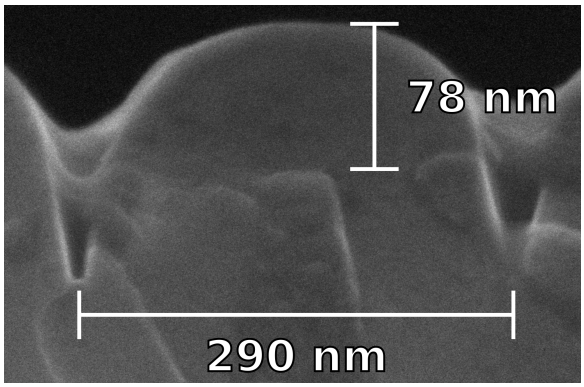

Figure 4.5: Cross-sectional SEM of conformally deposited Al_2O_3 over SiN_x nano-structures. The Al_2O_3 is the same thickness on the sidewalls and on top of the SiN_x tooth and the gap is beginning to fill in.

The conformal nature of the deposition only partially planarizes nano-structures (Fig. 4.5). For a true planarization, repeated planar dry etch and conformal deposition can be used, but will significantly increase the number of processing steps. Since

no additional lithography is required, this repeated process may be a useful option.

The final requirement for the dielectric fill of the EGC-LD is the ability to remove the hard mask above GaN p-contact surface. Usually, the procedure is to use an HF wet etch to remove an SiO_2 (or similar) hard mask layer. It is this requirement that renders many dielectric fill processes incompatible. For this reason, BCB was chosen instead of a conformally deposited dielectric.

4.5 Laser cavity mirrors

For edge emitting GaN LDs, the facet requirements are as follows: the facet should be vertical ($< 2°$ from normal); the facet roughness should be minimal ($< 5\,\text{nm}$); the facet face should be deep enough to interact with the entire optical mode. If possible, cleaved facets are by far the best option and are the preferred facet in commercial LDs.

However, some substrates like the semi-polar planes of GaN or devices bonded to substrates do not have a vertical cleave plane. The remaining options are then to lithographically mask and vertically dry etch the facet or to dice and polish back to the plane of the facet. In general, polished facets achieve the GaN facet requirements to higher degree than (ICP/RIE) dry-etched facets, but are more process intensive. [8]

4.5.1 Dry-etched facets

Many techniques for dry etching can be used to form facets. Reactive ion etching (RIE), chemically assisted ion beam etching (CAIBE), and the closely related focused ion beam milling (FIB) have all been used to etch vertical facets for GaN LDs. [9–11] In this work, we use RIE to etch $2\,\mu\text{m}$-deep facets for the AGC-LD.

An issue applicable to the general class of EGC-LDs is the etch memory effect on the facet surface. As seen in Fig. 5.9 (*top*), physical milling of a non-planar surface leaves streaks across the facet surface in the form of surface roughness, and will be present in all forms of dry etching. Though not quantified, the increase in roughness will decrease the nominal modal reflection. One partial solution to this issue is to slowly taper off the EGC towards the laser facet so that a standard ridge LD cross-section is used for the facet. Then, the scattering loss due to a rough facet can be avoided, at the cost of a more demanding lithography process.

4.5.2 Polished facets

To address the issues of a dry-etched facet, the EGC-LD device demonstration was made with polished facets, building off prior work at UCSB. [12] It was quickly discovered that fragile nano-structures of the EGC layer cannot withstand physical polishing. As seen in Fig. 4.6, the EGC layer breaks off and disrupts the polished surface. The resulting rough and non-uniform facet will result in increased scattering loss at the facet.

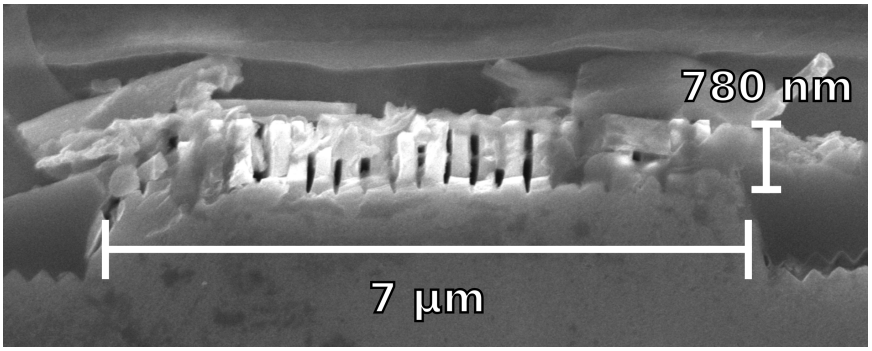

Figure 4.6: SEM of the polished facet of an EGC-LD.

Once again, the solution is to end the EGC layer before the facet plane in a non-

scattering fashion. This is more difficult with a polished facet because the facet plane is not easily fixed before-hand. An acceptable option may be to use a very shallow EGC layer so that the nano-structures are not as fragile, but the process is as yet untested.

4.5.3 Distributed Bragg reflector

The fabrication processes developed for the EGC-LD are well suited to producing a distributed Bragg reflector (DBR) or other photonic crystal effect. To make a DBR, the EGC structure should be rotated 90° and the pitch carefully controlled. For instance, a third-order DBR grating requires a pitch of approximately 270 nm, which is easily achievable with the fabrication processes described in this work.

A DBR LD design can replace dry-etched or polished facets for the purpose of optical feedback, but the issues of light extraction and prevention of unintended (disruptive) reflections remain. One straightforward option is to create a dry-etched or polished facet after the DBR. Then, to prevent disruptive reflections, one can either (a) anti-reflection coat the secondary facet and collect the light emission or (b) leave an unpumped region after the DBR to absorb the transmitted light. Implementation of such device designs is left to further work, leveraging the fabrication methods described here.

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Chapter 5

Device results

Laser diode devices utilizing a top etched-gap cladding (EGC) were designed based on the effective medium approximations and simulations described in **Ch. 2**. The goal of these devices was to demonstrate the effect of an EGC on the lasing mode.

The GaN-compatible fabrication techniques described in **Ch. 4** were applied to create the 1st generation of LDs with an air gap cladding and the 2nd generation of LDs with a BCB-filled etched gap cladding. The full process traveler for the 2nd generation EGC-LD is presented in *Appx. D.2*.

5.1 Air-gap clad laser diode device results

The air-gap clad laser diode was fabricated utilizing a compatible holography process (§4.1) to create 150 nm-wide trenches in GaN (300 nm pitch). An angled deposition of the Pd contact metal was used to seal the trenches and complete the

air gaps, as described in §4.4.1.

The epitaxial structure, simulation, and laser design are discussed before analyzing the LD device results. Based on detailed simulation, some device failure modes are explored and design improvements are proposed.

5.1.1 The epitaxial structure

Good laser diode design requires that the epitaxial structure and device geometry be designed together. The approach taken for the 1st generation was to try and balance the strong index contrast of the etched air-gap cladding at the top of the waveguide with an $Al_xGa_{1-x}N$ cladding at the bottom. Growth considerations limit the thickness and Al content of the $Al_xGa_{1-x}N$ layer, thus limiting the effectiveness of the bottom cladding. A layer that is too thick for the amount of Al in the layer will cause a break down in the growth morphology, even to the point of cracking the epitaxial film. [1]

The epitaxial growth was performed in a metal organic chemical vapor deposition reactor (courtesy of Dr. Kathryn M. Kelchner). Starting with a 300 µm bulk GaN *m*-plane substrate, the growth was as follows: a 2 µm Si-doped n-GaN layer ([Si] = $5 \times 10^{18}\,\mathrm{cm}^{-3}$), a 1.3 µm-thick n-$Al_xGa_{1-x}N$/GaN superlattice (SL, 36 periods, x = 10%, [Si] = $5 \times 10^{18}\,\mathrm{cm}^{-3}$) as the waveguideŠs lower cladding ($\Delta n = 0.02$ vs. GaN), an n-GaN waveguiding layer ([Si] = $5 \times 10^{17}\,\mathrm{cm}^{-3}$), an unintentionally doped (UiD) active region consisting of three 2.8 nm-thick QWs and four 14 nm-thick GaN barriers, an $Al_xGa_{1-x}N$ (x = 18%, [Mg] = $5 \times 10^{19}\,\mathrm{cm}^{-3}$) electron blocking layer (EBL), and a 50 nm low-doped p-GaN layer ([Mg] = $1 \times 10^{19}\,\mathrm{cm}^{-3}$). The top 500 nm of epitaxial growth are p-doped with stepped increases to make electrical contact ([Mg] = $\{2 \times 10^{19}, 4 \times 10^{19}, 6 \times 10^{19}, 2 \times 10^{20}\}$ cm^{-3} for {300, 25, 125, 20} nm) of which

the upper 275 nm is etched with air gaps.

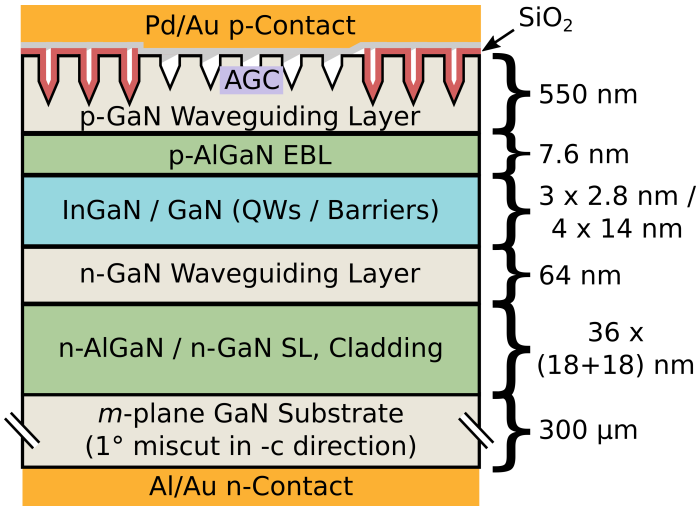

Figure 5.1: Schematic cross-section of 1st generation, air-gap cladding LD waveguide. Lasing direction is out of the page.

Experimentally, a super-lattice (SL) of thin, alternating layers of $Al_{0.1}Ga_{0.9}N$ and GaN (36 pairs, 18+18 nm) was found to be close to the growth limits while providing as thick and high index-contrast cladding layer as possible. Schematically, the waveguide structure is shown in Fig. 5.1.

5.1.2 Air-gap cladding etch profile and simulation

The periodic trenches in GaN that comprise the AGC are dry etched using the Unaxis etch tool & process described in §3.2.4. The resulting etch profile of each trench has nearly vertical sidewalls at the top, but a triangular bottom section (Fig. 5.2). Thus, the refractive index profile between the AGC at the surface and the GaN waveguiding layers is a continuous function. This fact is reflected in the 1-D waveguide simulation (Fig. 5.3).

Different sidewall and trench-bottom profiles can be achieved by varying the gas

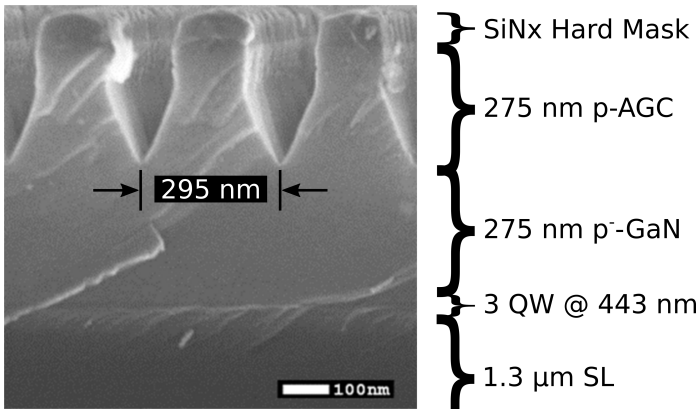

Figure 5.2: SEM micrograph of an LD ridge cross-section after the air-gap dry etch. Air-gap depths outside the ridge (the "field") are 50 nm deeper than in the ridge. Note the triangular shape of the AGC etch.

flow (either total flow or Cl_2:Ar ratio). The final profile used was the simplest achieved; other profiles tended to either undercut or produce a protruding mound at the very bottom of the trench. A protrusion would be highly undesirable as it would decrease the index contrast without providing any benefits. An undercut sidewall profile may be desirable, but is not explored here.

The waveguide design has GaN waveguiding layers, with the triple $In_{0.14}Ga_{0.86}N$ QW active region helping to center the mode, in addition to the upper AGC and lower super-lattice cladding layers which push the mode from top and bottom. Without the AGC on top, the Pd contact would act as the low-index cladding, but the mode would not be well centered on the active region (Fig. 5.3).

The bottom SL helps to contain the mode, but the index contrast of the AGC with GaN ($\Delta n = 1.17$) is much greater than the SL (if approximated as $Al_{0.05}Ga_{0.95}N$, $\Delta n = 0.02$). Therefore, the bottom evanescent tail of the mode penetrates quite deeply into the 1.3 µm SL and the mode shape is extremely asymmetric.

Fundamentally, this waveguide allows some of the modal power to "leak" into

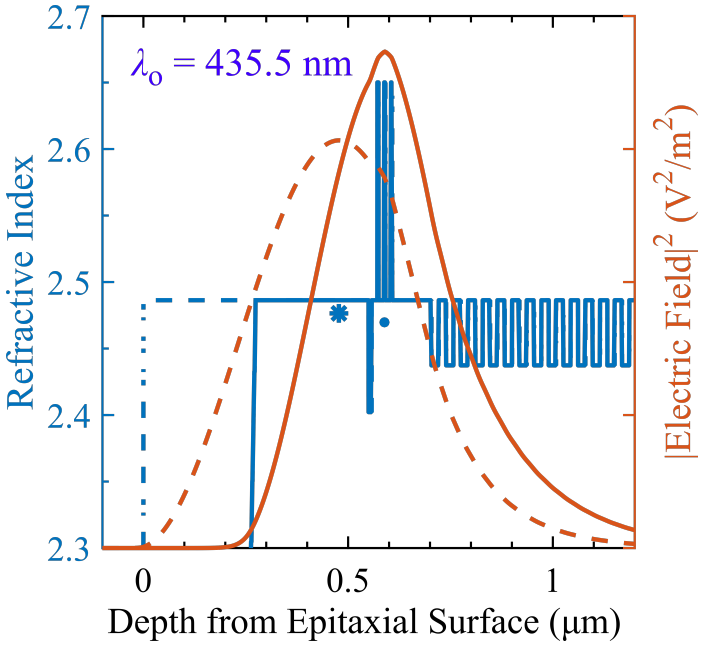

Figure 5.3: 1-D simulation of the mode profile (orange) given the refractive index profile (blue) with (solid lines) and without (dashed lines) the air-gap cladding. The corresponding modal effective index marked with a blue circle and star, respectively.

the substrate. Since the waveguiding layers are GaN, the optical mode will have an effective index in between that of GaN and the cladding; in this case, $n_{\text{eff}} - n_{\text{GaN}} = -0.017$. Therefore, the small amount of evanescent tail that leaks through the SL cladding will be a guided standing wave in the bulk GaN substrate. This results in the substrate acting as a waveguide that competes with the active region. As long as this leakage is small enough, the power residing in the substrate will be negligible. However, as explored in §2.2.3, while the relative electric field magnitude of the mode in the substrate is small, the thickness of the substrate allows a large portion of the modal power to reside in the substrate.

There are two approaches to mitigating mode leakage apart from thicker and/or higher index-contrast cladding. The first is to increase the index of the waveguiding layers so that the effective index of the mode is greater than index of the GaN sub-

strate. Then, GaN acts as a cladding layer itself. In the 2nd generation of EGC-LD devices, this is accomplished with 60 nm-thick $In_{0.065}Ga_{0.935}N$ layers on either side of the active region.

The second approach to mitigate mode leakage is to thin the layer that the mode leaks into. For instance, many GaN-based LD devices grown on sapphire substrates suffer from mode leakage into the initial GaN buffer layers, but because this layer is 1-10 µm thick, the fractional power of the mode leakage is negligible. Applying this method to bulk GaN LD devices means that the majority of the 300 µm-thick substrate should be removed in some fashion and replaced with a low index (i.e. $n < n_{\text{eff}}$) material.

5.1.3 AGC-LD device results

Two die repetitions of LD devices with ridge widths of 3 µm to 12 µm in increments of 3 µm and lengths of 300 µm to 1800 µm in increments of 300 µm were fabricated, for a total of 24 devices per die. The devices were tested under pulsed electrical injection on a thermoelectrically stabilized temperature stage. The amount of current required by these devices were often higher than the maximum output of the pulse generator ($\sim$ 1.8 A), scaling with the device area. Therefore, only the smaller ridge widths of 3 µm and 6 µm could be tested.

Electrically injected lasing at room temperature (stabilized at 20 °C) was achieved (λ = 435.5 nm) with a 0.25 µs pulse width and a duty cycle of 0.25%. An LD light-current (L-I) curve and series of spectra from a 6 µm × 300 µm device are shown in Fig. 5.4. The spectra narrowed considerably at current densities above the threshold current density (J_{th}) of 26 kA/cm^2, from 7.4 nm at 90% of J_{th} to 0.16 nm above J_{th}.

The temperature dependence of the device in Fig. 5.4 was evaluated at tempera-

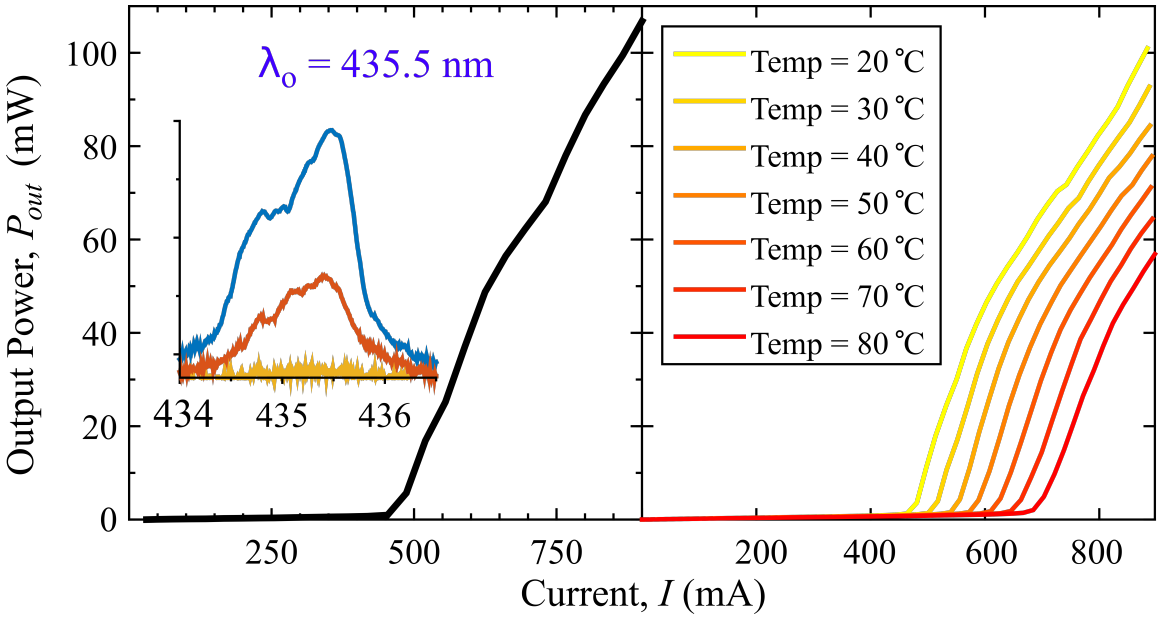

Figure 5.4: *Left* — L-I curve for a single facet of a 6 µm × 300 µm LD; $I_{th} = 475$ mA. Inset: spectra (x-axis: wavelength in nm; y-axis: intensity, log scale in decades, a.u.) from bottom to top: {0.99, 1.01, 1.1} $\times I_{th}$. *Right* — L-I curves for varied stage temperature.

tures $\geq 20\,^{\circ}$C. The characteristic temperature, T_o, was determined to be 152 K. This is comparable to a previously published T_o for a blue m-plane LD of 156 K. [2]

The J_{th} and differential efficiency (η_d) from a single facet of the device in Fig. 5.4 were 26 kA/cm^2 and 8.25%, respectively. However, these results were not consistent among the other devices tested. Fig. 5.5 shows the J_{th} of the lasing devices vs. length. The results do show the known trend of reduced threshold current density with length, but the data points are too few and varied to draw conclusions about the other internal device parameters such as internal loss.

Similarly, η_d did not display a consistent enough trend to draw conclusions about the internal device parameters.

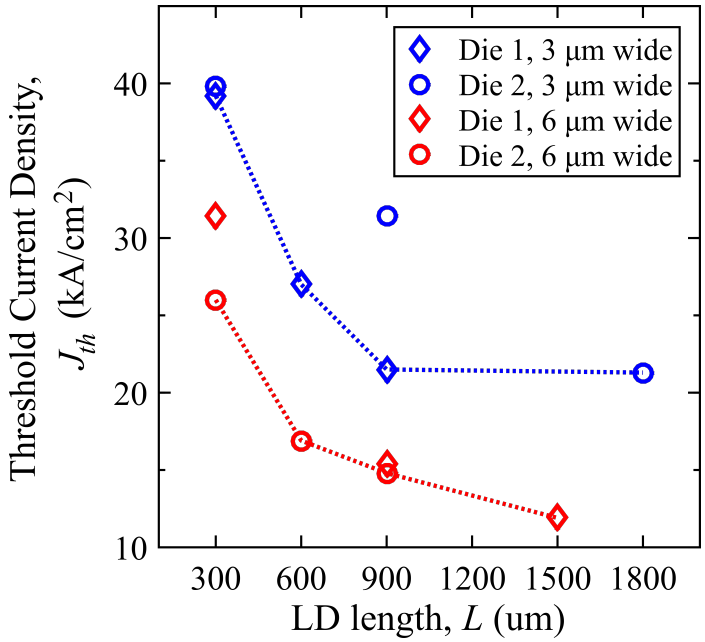

Figure 5.5: Threshold current density vs. length for all AGC-LD lasing devices.

5.1.4 AGC-LD failure analysis

The most evident failure mode of the AGC-LD devices by visual inspection was the delamination of the top contacts. Many of the top metal pads peeled away from the substrate, causing an open circuit condition on 50% of the devices. The angled metal deposition seemed to deposit a film under more stress and/or less adhesion than previously observed. It is not known whether the angled nature is part of the issue. A very likely factor in the delamination is the change in e-beam deposition tool — this was necessary to accommodate the angled fixture. However, the new deposition tool does not achieve as low a base pressure which can reduce adhesion of the deposited film.

The p-contacts also exhibited non-ohmic behavior. The linear transmission line method (TLM) test structures showed non-linear current-voltage relationships, indicating that the Pd contact metal has a significant electrical barrier to the p-GaN; the

above-threshold series resistance was about 5.2 Ω. This explains the relatively high threshold voltage of ∼ 11 V, compared to typical threshold voltage results of 6 V to 8 V for similar epitaxial growths. It cannot be determined from the devices or test structures whether the fabrication process for the AGC plays a role in the p-contact quality.

The J_{th} is also higher than anticipated, in addition to its large variation. A high threshold voltage also leads to higher threshold current simply due to the increased operating temperature, though this effect is greatly mitigated under pulsed-current test conditions. Therefore, unexpected optical mode profiles (e.g. mode leakage) likely play a bigger role.

The mode leakage into the substrate has a two-fold effect on the lasing mode. First, the more power that resides in the thick substrate, the less power is guided in the main waveguide, reducing the confinement factor in the gain material. Reduced confinement factor directly leads to increased threshold current.

The second effect is that the mode power in the substrate will not be reflected by a 2 µm-deep etched facet mirror, causing the unreflected power to be lost from both the waveguide and lasing outpu. This parasitic loss significantly increases the total loss, again increasing the threshold current. In addition, parasitic loss reduces the light output after lasing has been achieved, resulting in a lower η_d.

The amount of mode leakage is difficult to determine with accuracy. It is very sensitive to thicknesses of the waveguide layers, including the etch depth and fill fraction of the AGC. Through simulation, the mode leakage is hypothesized to be between 10% and 40% of the total modal power, and may vary between devices on chip. This also means that the modal confinement factor may vary by the same amount. This variation makes it difficult to determine extrinsic modal parameters

like total loss, and may be the main confounding factor when analyzing the measured data.

5.2 Etched-gap clad laser diode device results

The full process traveler for the 2nd generation, EGC-LD is given in *Appx. D.2*. The fabrication process includes a number of new process steps, including an initial Au-Au bond to a silicon substrate, e-beam lithography to pattern the EGC, and a spin-on BCB fill to complete the EGC.

Bonding to a Si substrate adds a significant number of steps on the front end of the process, but allows for much easier handling of small bulk GaN substrates and better utilization of the chip surface area. This is particularly apparent in the case of e-beam lithography — the mounted m-plane substrate is patterned with a die that is 4.5 mm tall. An unmounted chip would be restricted to 3 mm due to the limited mounting options in the particular e-beam lithography tool used.

Additionally, the Si substrate adds much needed mechanical robustness at the end of the process when the wafer is diced into long, narrow laser bars of $\sim 20\,\text{mm} \times 0.6\,\text{mm}$ in surface area and polished on edge. In the final testing stage, the bonded Si substrate acts as both the backside n-contact and a heatsink without the need for further mounting or manipulation of the fragile laser bars.

5.2.1 The epitaxial structure, 2nd generation

For the 2nd generation of devices, the goal is to compare LD devices with and without an EGC. The comparison should have as many commonalities as possible to isolate the feature of interest. Therefore, the epitaxial design must accommodate both

LD geometries reasonably well, and both designs must be fabricated simultaneously on the same wafer. In doing so, neither design will be optimized for device performance.

Building off of the learning from the 1st generation, the epitaxial structure now focuses on a high index waveguiding layer to eliminate any competing waveguide and mode leakage in the bulk m-plane substrate. Symmetric n-side and p-side $In_{0.065}Ga_{0.935}N$ layers (each 60 nm thick) act as the waveguiding layers, for an index contrast of $\Delta n = 0.06$ with the lower GaN cladding, and $\Delta n = 0.65$ with the upper EGC. Thus, the optical mode will be anchored in the waveguiding layer, but the evanescent wings will be highly asymmetric and push deeper into the lower n-side.

The latest iteration of the three-QW blue (451 nm) active region is utilized (MOCVD growth courtesy of Leah Y. Kurtizky). In-house experiments show that the AlGaN electron blocking layer is no longer needed and has since been removed from the growth. In between the waveguiding layers, the active region consists of four 10 nm-thick UiD GaN barriers and three 4.6 nm-thick $In_{0.16}Ga_{0.84}N$ QWs.

The waveguiding layers surrounding the active region contain a significant portion of the mode field intensity. To limit the modal absorption, the p-waveguiding layer is doped with $[Mg] = 1 \times 10^{19}\,cm^{-3}$ and the n-waveguiding layer is doped with $[Si] = 1 \times 10^{18}\,cm^{-3}$. It is not clear if these doping concentrations can be reduced further without incurring prohibitive electrical losses, though the reduction in modal absorption is clear.

5.2.2 Etched-gap clad device fabrication and simulation

When comparing the 1-D mode profile of an EGC-LD and a ridge LD, it is clear that EGC will push the mode down, but may also expand the mode below the ridge. For a shallow ridge LD, this means that the mode will tend to "flatten out" hori-

zontally, making the effective width of the mode very different when comparing the EGC-LD and shallow ridge LD. As a consequence, the injection efficiency and modal absorption would be different between the two designs.

Thus, a simplified goal of these two waveguide designs is to create different vertical profiles, but similar horizontal profiles. A deep ridge design that is etched through the waveguiding layers will laterally confine both modes in a similar manner, regardless of the top cladding. Now, the injection efficiency can be assumed to be the same for both the EGC-LD and deep ridge LD.

To create the vertically asymmetric mode (Fig. 5.6), the EGC must be etched quite close to the waveguiding layer. In addition, the p-GaN in which the EGC is etched must be quite thick (750 nm), making the EGC a deep etch. This is because the purpose of this epitaxial design is to provide reasonable device performance *without* the EGC as well.

Table 5.1: 1-D simulation comparison of the EGC-LD and ridge LD.

Parameter	EGC-LD	Ridge LD
n_{eff}	2.4738	2.4811
κ (10^{-5})	4.56	7.59
α_{EV} (cm^{-1})	12.717	21.152
α_{Ov} (cm^{-1})	12.716	21.151
Γ_{InGaN}	4.18%	4.16%

Thus, the fabrication demands for these devices are much harder than the 1$^{\text{st}}$ generation. The hard mask for the EGC must withstand at least 750 nm of GaN etching. This is not possible with the previously used holography process.

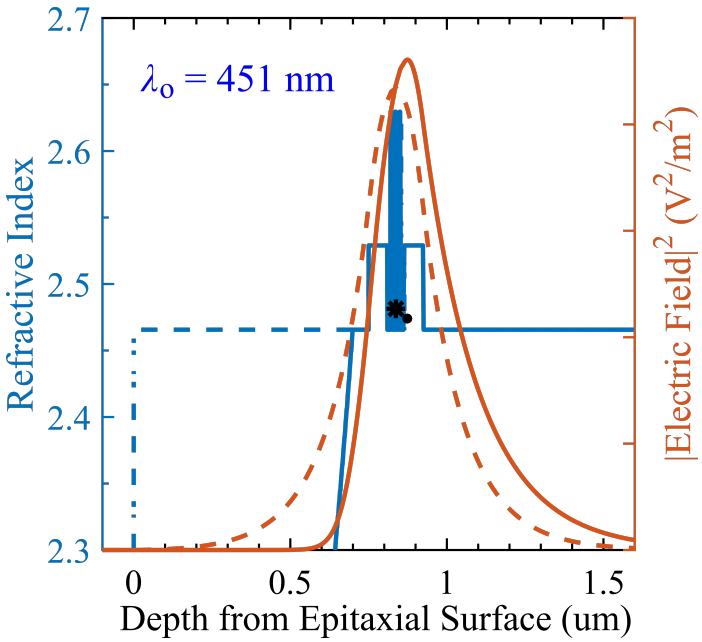

Figure 5.6: 1-D simulation of the mode profile (orange) given the refractive index profile (blue) with (solid lines) and without (dashed lines) the etched-gap cladding. The corresponding modal effective indices marked with a black circle and star, respectively.

Instead, the electron beam lithography process can accomodate much thicker etch depths. The lifted-off thin (30 nm - 40 nm) Ni hard mask can then be used to etch a thicker ($\sim$ 500 nm) SiO_2 hard mask. This dielectric hard mask can now be used to etch the GaN (Fig. 5.7.a).

The Ni hard mask was considered as a possible mask for the GaN etch, but was found to be incompatible. The thin Ni layer does act as a high selectivity hard mask for the GaN. In general, a thin patterned mask causes less shadowing and less chemical transport issues during dry etch, leading to more repeatable and uniform etch profile. However, the thin Ni layer contributed to the formation of a chemically resistant residue that filled the trenches of the EGC in-situ (Fig. 5.7.b). Instead, the Ni mask was removed via wet etch between the SiO_2 etch step and GaN etch step,

leaving the patterned SiO_2 to mask the GaN.

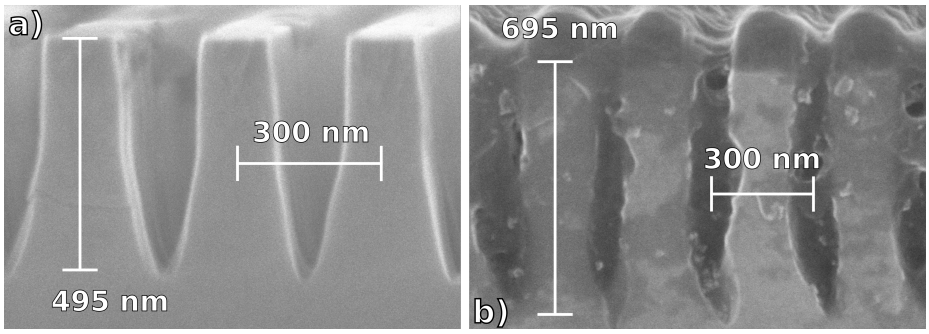

Figure 5.7: SEM cross-section of patterned GaN dry etch: **a)** using an SiO_2 hard mask only (hard mask has been removed); **b)** using an SiO_2 + Ni hard mask (unable to remove hard mask/residue).

While these process steps are still useful, it is much preferable to have a thin p-GaN layer and a shallower etch. In a device design optimized for an EGC, this can be accomplished with a ~ 100 nm-thick EGC layer. Then, the most significant role of the EGC is to act as an optical barrier to metal absorption, rather than reducing optical absorption in Mg-doped GaN. This design shift is further reinforced as doping concentrations around the active region are reduced. The optical benefits (lower absorption, higher confinement factor) are still apparent (Table 5.1), but are not as significant after the overall material absorption is reduced. However, the decrease in series resistance after thinning the p-GaN is another possible, but untested benefit.

5.2.3 EGC-LD device results

The final devices were diced into three uniform laser bars of 600 µm, 900 µm, and 1200 µm. All devices were fixed at 6 µm wide. There were eight repetitions of EGC-LDs and ridge LDs per die, per laser bar. Nearly four die fit on the wafer for a total of 60 devices per laser bar.

For a select few devices, electrically injected lasing was achieved ($\lambda_o = 451\,\text{nm}$) at a pulse width of 0.5 µs and a duty cycle of 0.5%. The lasing devices were spatially located in exactly the same position on each die and happen to be non-EGC deep ridge LDs. The majority of devices were found to be electrically shorted, including all the EGC-LDs. The light-current-voltage curve of a lasing 6 µm × 600 µm deep ridge LD is given in Fig. 5.8.

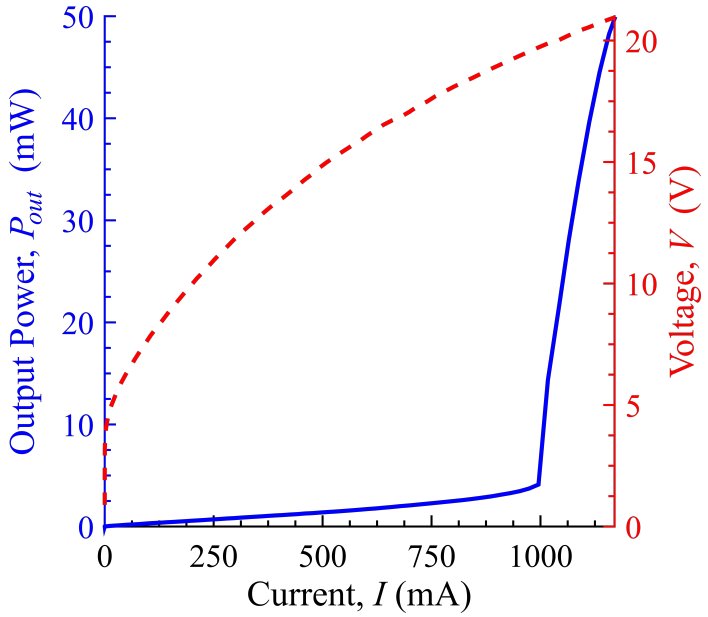

Figure 5.8: Light-current-voltage plot from one facet of a 6 µm × 600 µm deep ridge LD lasing at 451 nm. At threshold, $J_{th} = 27.8\,\text{kA/cm}^2$, $V_{th} = 19.7\,\text{V}$, and the differential resistance is 7.4 Ω.

5.2.4 EGC-LD failure analysis

All devices exhibited high differential resistance across the entire I-V sweep. The I-V curves of the shorted devices resembled that of a high resistance wire rather than a diode, while lasing devices exhibited diode behavior with large differential resistance

at high currents. All the devices tested emitted spontaneous emission, meaning that the junction itself performed as expected and likely did not contribute to the electrical short.

A likely cause of the shorting is a metal shunt path along the sidewall of the deeply etched ridge. If a deep ridge waveguide is not properly isolated with a dielectric, the top contact metal can directly short the p-n junction. After fabrication, it was observed that the solvent 1165 caused the BCB dielectric to swell and detach from the GaN. To investigate this hypothesis, destructive cross-sectional cuts of the EGC-LDs and deep ridge LDs were performed to see if the spin-on BCB dielectric pulled away from ridge.

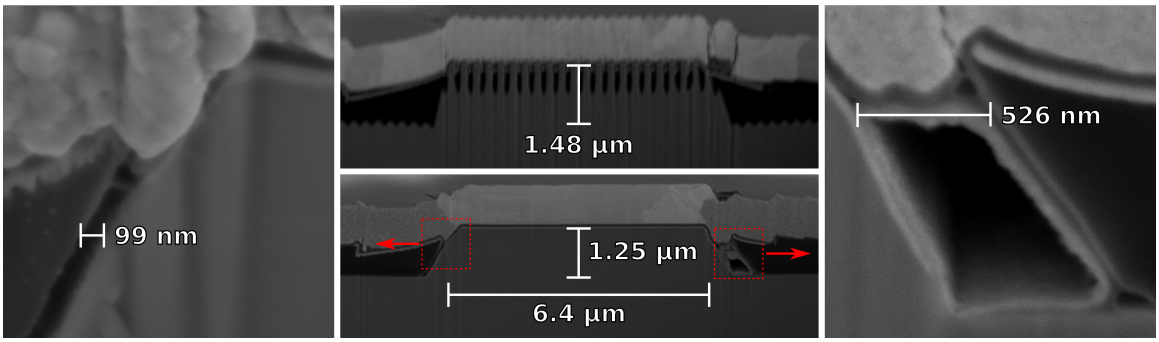

Figure 5.9: Cross-sectional FIB and SEM of (*top*) an EGC-LD ridge; (*bottom*) a deep ridge LD; (*left*) slightly delaminated BCB from left side of the deep ridge LD; (*right*) large delamination pocket from right side of the deep ridge LD. *FIB & SEM courtesy of Charles Forman.*

Cross-sectional SEMs of an EGC-LD and a ridge LD are shown in Fig. 5.9. The focused ion beam milling to create the cross-section was performed by Charles Forman at the California NanoSystems Institute, UC Santa Barbara, allowing us to look at the final devices geometry.

A few new details about the fabrication process are evident. First, it is clear that

the BCB did pull away from the ridge sidewall in some places, leaving large voids that could easily allow for an electrical short. Second, the EGC seems to be over-etched, possibly penetrating through the active region itself.

Both of these fabrication issues have straight forward solutions. In the case of BCB, the solvent 1165 should be avoided. Instead, compatible processes using acetone should be substituted. To avoid over-etching the EGC, the corresponding dry etch must be made more repeatable. The simple solution is to shorten the designed etch depth. Another possible fix is to greatly increasing the chamber loading to have slower, more repeatable etch rates, then carefully re-calibrate the etch.

Finally, it was noted that the linear TLMs on both EGC and non-EGC p-GaN showed extremely non-ohmic behavior. This means that the e-beam deposited palladium did not make good metal contact to the p-GaN, regardless of the presence of the EGC structure. Therefore, even if the threshold current density were in the $10\,\mathrm{kA/cm^2}$ range, the threshold voltage would still be around $11.8\,\mathrm{V}$.

It is currently unknown whether the bad contact is due to an epitaxial issue or a fabrication issue, though in both cases well-used process parameters and machines were employed. A p-contact first approach may mitigate this issue, but is beyond the scope of this work.

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Chapter 6

Conclusions & future work

We have demonstrated a dry etch process that is useful for producing lithographically defined surface-etched features close to the active region of GaN-based light emitters. The deleterious effect of sub-surface etch damage on the η_{IQE} of c-plane InGaN/GaN QWs was evaluated using a double-active region structure for calibrated PL measurements. No damage was observed for an etched surface that is 71 nm from the top most QW. The onset of sub-surface etch damage occurred between 71 nm and 25 nm, after which severe deterioration of the η_{IQE} was observed.

As a demonstration of new design applications, this dry etch process was used to produce a 150 nm-wide, 300 nm-spaced air gap pattern that acted as a waveguide cladding of an m-plane InGaN/GaN LD. We achieved room temperature lasing at 435.5 nm under pulsed electrical injection.

A 2$^{\mathrm{nd}}$ generation of devices was fabricated with fabrication process versatility in mind. An etched-gap cladding was patterned using a direct-write electron beam lithography process, then filled with spin-on BCB dielectric. Both EGC and standard

ridge design lasers were fabricated on a single wafer. In doing so, we developed a new way to accomplish deeply etched, low line edge roughness (LER) features on GaN using electron beam lithography.

The learning obtained from these devices is summarized in §6.1.1 as a cohesive group of design principles for future EGC-LDs. While the majority of EGC fabrication process has been worked out, the full role of EGCs in GaN LD design has yet to be explored.

Furthermore, the combined process development of a low-damage dry etch and low-LER, deeply etched features opens up a new design flexibility in fabrication process flows and GaN device design. Therefore, the process tools developed in this work have uses beyond etched-gap cladding for laser diodes.

6.1 Next generation EGC-LDs

A small amount of process development for EGC-LDs remains. The conclusions drawn from the 1st and 2nd generation LD devices give a clear road-map for future EGC-LDs. None of the conclusions require new fabrication steps, only further device demonstration to confirm the design principles learned.

With these principles in mind, we can explore the possibility of combining the EGC with another low-index cladding option, transparent conductive oxides (TCOs). Furthermore, we can look to make more complicated designs integrating photonic crystals (PhCs) like distributed Bragg reflectors (DBRs) with almost no change to the fabrication process.

6.1.1 Continued process development for EGCs

Reviewing the device results and failure analysis from the 1st and 2nd generation LDs, we can summarize a list of conclusions for waveguide design. First, the low index of an EGC will greatly lower the effective index of a mode and will result in mode leakage into GaN if unchecked. Therefore, $In_xGa_{1-x}N$ waveguiding layers are recommended to ensure a modal effective index greater than the (GaN) substrate. A lower $Al_xGa_{1-x}N$ cladding can still be used if growth techniques allow it, but is not sufficient on its own. If instead a low-index cladding on par with an EGC can be utilized, high-index waveguiding layers may not be necessary.

Second, the EGC should be considered an efficient barrier to mode penetration first and foremost. In other words, a thin EGC layer above a thin waveguiding layer ($\sim$ 100 nm each) can be used to prevent the mode overlap with optically lossy top metal contacts. In conjunction with low-doped Mg:GaN layers, this has a slight optical benefit of reducing modal loss and increasing modal gain, though these can be thought of as secondary benefits. With a much thinner p-type cladding layer, one should see a significant reduction in series resistance, though this is yet to be demonstrated.

Third, a timed, deep dry etch of GaN using the developed low-damage process is not repeatable enough to accommodate the layer thickness tolerance required of an EGC. Instead, the EGC should be as thin as possible while still providing an adequate cladding layer. As a processing tool, a deep, low-damage etch is still possible in situations where the process tolerance is not as tight.

Finally, while a deep ridge design is possible with the developed process, a shallow ridge design that does not etch through the active region carries less risk of fabrication error. Furthermore, the fabrication process is greatly simplified if the ridge and EGC

are patterned simultaneously via electron beam lithography, thus requiring a single etch step. However, in some instances the deep ridge design did lase despite adhesion issues with the BCB dielectric, showing that the deep ridge LD design for GaN may be a viable design. Optically and electrically, the mode should have better confinement; a robust process for deep ridge LDs in GaN is worth further investigation.

Regardless of ridge etch depth, future process flows using BCB should avoid the use of the 1165 solvent once BCB has been applied; in fact, further testing is required to determine which solvents (other than acetone and isopropyl alcohol) are compatible with BCB. In instances requiring planarization and process compatibility with SiO_2 layers, the benefits of BCB out-weigh the trade-offs.

6.1.2 Combining an EGC with indium tin oxide

Transparent conductive oxides (TCOs) can provide a similar index contrast cladding layer to an EGC. It functions both as the top p-contact to GaN as well as the conductive cladding layer. However, the optical loss is usually quite high, but still much lower than metal losses. For example, indium tin oxide (ITO), a well-explored TCO for GaN light emitters, can have up to an order of magnitude higher absorption than the p-GaN with which it makes contact. [1]

TCOs also require a different process flow than a normal metal contact. The standard process flow for ITO is to perform a blanket deposition, then lithographically pattern and dry etch the ITO and GaN. Since the ITO can be dry etched, it can be integrated into the EGC process flow itself. Then the EGC would be comprised of GaN and ITO.

The benefits of an ITO+GaN EGC are many. The final structure is a very efficient cladding layer. Both the ITO and GaN can be very thin ($< 50\,\text{nm}$ each), while still

maintaining a low optical loss cladding. The process tolerance for such a short GaN dry etch is well within most waveguide design requirements. A p-contact first approach can be adopted to achieve ohmic contacts. With further process development, this new EGC could be the next generation of EGC-LDs.

6.2 Beyond EGCs

The developed fabrication process allows for a wide variety of etched geometries close to active layers in GaN-based devices. We have shown that it can be used to create electrically conductive high index-contrast layers for optical devices. Comparable low optical loss, high index-contrast claddings have not been demonstrated by other growth or fabrication means in GaN-based devices, making it especially useful for the next generation of high performance short wavelength laser diodes.

A further application of this process is etched PhCs. For LEDs, PhCs provide a means of light extraction of guided modes. [2] For LDs, PhCs can either be used for light extraction, or as a reflecting feedback element in a cavity. [3–5] For example, LDs with grating lines of appropriate width and pitch oriented perpendicular to the lasing direction can form a distributed Bragg reflector (DBR). With detailed waveguide engineering, a sub-wavelength pattern can serve as both cladding and minimally-coupled grating for distributed feedback (DFB) LDs. As with the demonstrated LD design, these structures still maintain electrical conductivity and active region integrity.

6.2.1 Surface etched PhCs in GaN LEDs

In the case of LEDs, enhanced light extraction can be achieved via etched PhCs. Previously demonstrated devices [6] required a regrowth to place low-loss, conductive PhCs near ($\sim 150\,\mathrm{nm}$ from) the active region. Their goal was 2-fold. First, the etch damage to the η_{IQE} induced by their dry etch was severe; a regrowth of material in an MOCVD chamber was sufficient to recover most (but not all) of the active region performance. [6] In fact, in-house experiments of a high-temperature anneal $\sim 900°$ with an ammonia overpressure in the MOCVD reactor (no actual material growth) was sufficient to partially recover the damage.

Second, they wanted to coalesce the film to utilize the full surface area. If the PhC were below the active region, this means that the subsequently grown active region volume would be undiminished. Above the active region, the coalescence of the p-type material allowed for metal contact to the entire surface, rather than a fraction equal to the GaN fill factor.

By employing the etch process described in this work, PhCs can be applied in both as-grown and flip-chip orientations without regrowth. Furthermore, the PhCs could be placed much closer to the active region, which was an explicit desire of Jewell *et al.* [6] to achieve better light extraction. Therefore, many new design options are now feasible. The process compatibility of the demonstrated etch process makes it a valuable tool when etched features are required near damage-sensitive layers in III-Nitrides.

6.2.2 Combining EGCs and Bragg gratings

The electron beam lithography process for EGCs was developed with photonic crystals (PhCs) in mind. The design flexibility of e-beam lithography easily accommodates PhCs like a 1-D Bragg grating. For instance, a third order grating at 450 nm requires a pitch of ~ 270 nm in GaN, oriented along the lasing direction. This is very close to the standard 300 nm pitch used throughout this work, but rotated by 90°.

In designing such features for use in an LD device, it is important to keep in mind that the EGC consists of high index contrast layers of GaN and dielectric. As a top etched feature, these high index contrast layers cannot be used directly to create the grating. Alternating layers of GaN and dielectric would cause large scattering at each interface, leading to unacceptable optical losses.

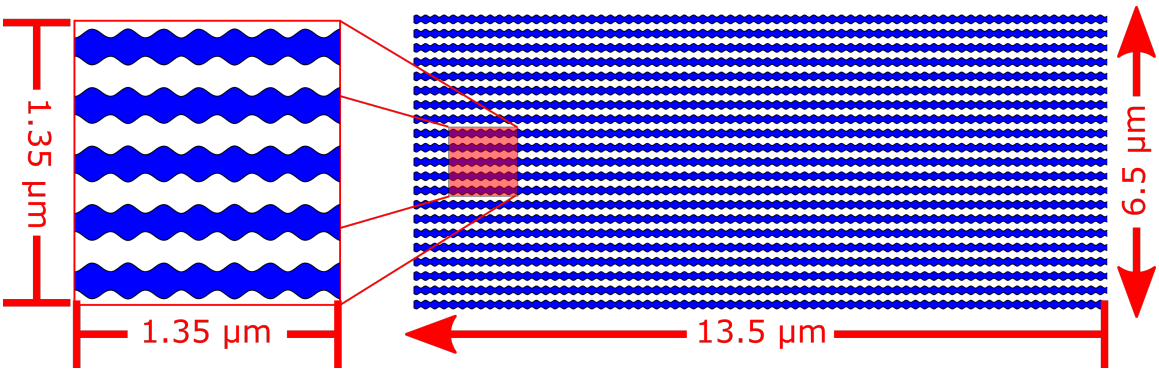

Figure 6.1: Top-down schematic of a (shallow ridge) EGC waveguide with a 1st order grating ($\Lambda = 90$ nm) for a GaN-based LD at $\lambda = 450$ nm. The original EGC pattern is modulated with a sinusoid to produce an integrated, low scattering-loss DBR.

Instead, the EGC can be slightly modified from its current form to approximate a low-index contrast grating. Rather than changing the orientation of the etched trenches, a smooth sinusoidal modulation can be applied to the trenches at the desired pitch (Fig. 6.1). Electron beam lithography can easily accommodate the change,

while all other processing remains the same. Furthermore, even a 1st order grating ($\sim 90\,\text{nm}$) can be fabricated without any processing compatibility issues.

A mirror made using a low-loss, surface-etched grating is a powerful design element for semiconductor LDs. Eliminating one or both of the mirror facets can simplify back-end device processing, lowering both the fabrication risk and fabrication cost. For instance, with a highly reflective DBR, manipulating a laser bar to coat the edge with a dielectric mirror is no longer needed. Furthermore, an etched DBR allows for on-chip optical device integration, opening the door to an entirely new field for GaN optoelectronics.

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Appendix A

Optical material properties

The optical properties of the $(Al_x,In_x)Ga_{1-x}N$ material system are constructed from a few sources, spanning both experimental data and theoretical calculations. While the absolute value of these properties is important for accurate optical mode simulations, the relative values are even more so. Therefore, a large emphasis is placed on consistency for determining a particular property across varying alloy content and wavelength.

Properties of other materials like dielectrics and metals are easier to obtain. Additionally, they have less of an influence on the optical mode simulations of this work, so the accuracy requirement is more relaxed.

A.1 Bandgap of (Al,In)GaN

GaN — the bandgap determined by Sakalauskas *et al.* [1] is used:

$$\text{GaN}: \; E_g = 3.435\,\text{eV}, \; \lambda_g = 360.9\,\text{nm} \tag{A.1}$$

$Al_xGa_{1-x}N$ — the bandgap determined by Buchheim *et al.* [2] is used, valid for up to 50% Al content. For consistency, the bandgap of GaN determined above is utilized. The effect of strain is not considered.

$$Al_xGa_{1-x}N\colon\ E_g = x\cdot E_{g,\mathrm{AlN}} + (1-x)\cdot E_{g,\mathrm{GaN}} + x(1-x)\cdot E_b \tag{A.2}$$

$$\mathrm{AlN}\colon\ E_g = 6.16\,\mathrm{eV},\ \lambda_g = 201.3\,\mathrm{nm} \tag{A.3}$$

$$Al_xGa_{1-x}N\ \text{bowing}\colon\ E_b = 0.9\,\mathrm{eV} \tag{A.4}$$

$In_xGa_{1-x}N$— the bandgap is determined using the work of Sakalauskas *et al.* [1] In this equation of bandgap vs. In content, x, the effect of a fully strained layer is considered. The equation for strain is valid over the In content range of 0% - 20%.

$$In_xGa_{1-x}N\colon\ E_g = x\cdot\left(E_{g,\mathrm{AlN}} + E_s\right) + (1-x)\cdot E_{g,\mathrm{GaN}} + x(1-x)\cdot E_b \tag{A.5}$$

$$\mathrm{InN}\colon\ E_g = 0.675\,\mathrm{eV},\ \lambda_g = 1837\,\mathrm{nm} \tag{A.6}$$

$$In_xGa_{1-x}N\ \text{bowing}\colon\ E_b = 1.65\,\mathrm{eV} \tag{A.7}$$

$$In_xGa_{1-x}N\ \text{strain}\colon\ E_s = 0.79\,\mathrm{eV} \tag{A.8}$$

In the case of $In_xGa_{1-x}N$, the bandgap is used in the determination the refractive index.

$(Al_x,In_x)Ga_{1-x}N$ — to compare the ternary III-nitrides, we plot the bandgap vs. alloy content of $Al_xGa_{1-x}N$ and $In_xGa_{1-x}N$.

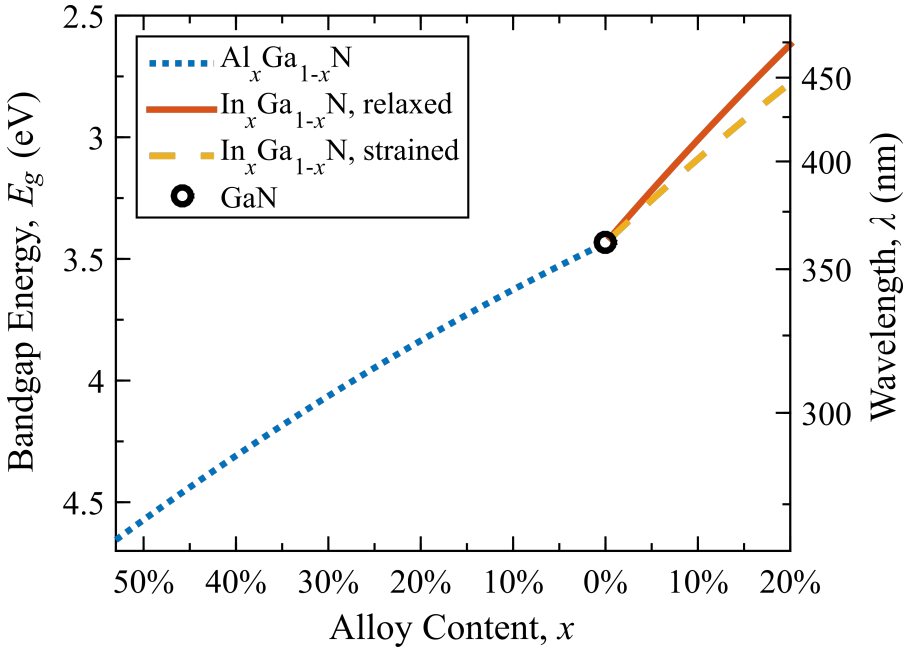

Figure A.1: Bandgaps for GaN, $In_xGa_{1-x}N$ and $Al_xGa_{1-x}N$.

A.2 Dispersion curves of (Al,In)GaN

LD simulations require a good approximation of the refractive indices, $\tilde{n}$, of constituent materials. At wavelengths sufficiently longer than the bandgap wavelength, the Sellmeier Equation (Eq. A.9) provides a good fit of the real refractive index, n.

$$[n(\lambda)]^2 = A + \sum_m \frac{B_m \lambda^2}{\lambda^2 - (C_m)^2} \tag{A.9}$$

where A is the long-wavelength dielectric constant, B is a weighting factor (unitless), and C [µm] is the absorption resonance frequency. These coefficients are always determined experimentally and are generally valid for wavelengths at or longer than the probe wavelengths. They are not valid in wavelength ranges of high absorption, such as near or shorter than the band gap wavelength of a semiconductor.

The refractive indices of GaN and $Al_xGa_{1-x}N$ vs. wavelength have been explored experimentally, while that of $In_xGa_{1-x}N$ is mostly theoretical. [3] Though data is

available for $In_xGa_{1-x}N$ over various In composition and wavelengths, [1,2] it is either over too sparse a wavelength range or suffers from large experimental error.

We fit an m-term Sellmeier Eqn. (Eq. A.9) for wavelengths equal to longer than the probe wavelengths in experimental data. For shorter wavelengths (e.g. near bandgap), we take a modification of measured data, as this is accurate enough for our purposes.

GaN — we fit the Sellmeier coefficients given in the work of Sanford *et al.* for both GaN and AlGaN to maintain consistency (Table A.1). The short wavelength coefficient A is fixed at 1. The birefringence is accounted for by considering the orientation of the electric field vector with respect to the **c**-axis of the wurtzite GaN crystal: perpendicular is labeled "ordinary" and parallel is labeled "extraordinary".

Table A.1: Sellmeier Coefficients for GaN (valid for $360.9\,\text{nm} < \lambda < 2500\,\text{nm}$).

Refractive Index	B_1	C_1 (nm)	B_2	C_2 (nm)
n_o	4.0848	179.19	0.0873	354.73
n_e	4.3172	189.63		

For wavelengths shorter than the probe wavelength of $0.442\,\mu\text{m}$, we use the data given in Bergmann *et al.* [4] (digitized from plot on p. 1197), with the index slightly shifted to make a continuous function.

$Al_xGa_{1-x}N$ — we fit a quadratic to the Sellmeier coefficients vs. Al content, x, given in Sanford *et al.* [5]

Table A.2: Quadratic fit to Sellmeier Coefficients vs. Al content (x) (valid for $0 < x < 60\%$ and $360.9\,\text{nm} < \lambda < 2500\,\text{nm}$).

Refractive Index	B_1	C_1 (nm)	B_2	C_2 (nm)
	4.0848	179.19	0.0873	354.73
n_o	-1.3986 x	-90.146 x	0.374 x	-299.29 x
	0.4056 x^2	49.158 x^2	0.2996 x^2	82.844 x^2
	4.3172	189.63		
n_e	-1.1473 x	-50.439 x		
	0.2906 x^2	-15.444 x^2		

The work of Rigler *et al.* [6] is also quite good, producing very uniform data between the wavelengths of 458 nm and 1064 nm. It is similar to the data of Sanford *et al.*, but tends towards a lower value of refractive index. However, the wavelength range investigated is farther from wavelengths of interest of this work ($< 450\,\text{nm}$). Therefore, we use the Sellmeier fits of Sanford *et al.*, but provide a quadratic fit for 2-term Sellmeier coefficients in Rigler *et al.* (with $A = 1$) below for completeness.

Table A.3: Quadratic fit to Sellmeier Coefficients vs. Al content (x) (valid for $0 < x < 60\%$ and $360.9\,\text{nm} < \lambda < 2500\,\text{nm}$).

Refractive Index	B_1	C_1 (nm)
	4.1725	182.58
n_o	-1.208 x	-66.91 x
	0.8127 x^2	-49.352 x^2
	4.3005	193.76
n_e	-0.8312 x	-125.19 x
	-0.6839 x^2	198.61 x^2

Again, as we near the band edge, we must supplement the Sellmeier coefficients with data from Bergmann *et al.* The measured dispersion curve of GaN is used as the basis, but shifted by the energy difference of the bandgaps and shifted in index to form a continuous curve.

$In_xGa_{1-x}N$ — using the technique of Bergmann *et al.*, [4] the full dispersion curve of GaN is used as the basis for the dispersion curve of $In_xGa_{1-x}N$, but shifted by the energy difference of the bandgaps. The validity of this method was further explored by Laws *et al.* [3] The valid In content range is 0% - 20% (limited by the bandgap calculation of the strained layer). Using the constants $h{\cdot}c_0 = 1239.8\,\mathrm{eV}{\cdot}\mathrm{nm}$ to convert between wavelength and energy, we have:

$$\begin{aligned} \mathrm{In}_x\mathrm{Ga}_{1-x}\mathrm{N}\colon\ & n_{\mathrm{InGaN}}(x,\lambda) = n_{\mathrm{GaN}}(\lambda') \\ & \lambda'(\lambda) = hc_0\left[\frac{h\,c_0}{\lambda} - \Big(E_{g,\mathrm{GaN}} - E_{g,\mathrm{InGaN}}(x)\Big)\right]^{-1} \end{aligned} \tag{A.10}$$

$(Al_x,In_x)Ga_{1-x}N$ — to compare the ternary III-nitrides, we plot the dispersion curves of $Al_xGa_{1-x}N$ and $In_xGa_{1-x}N$ with varying composition.

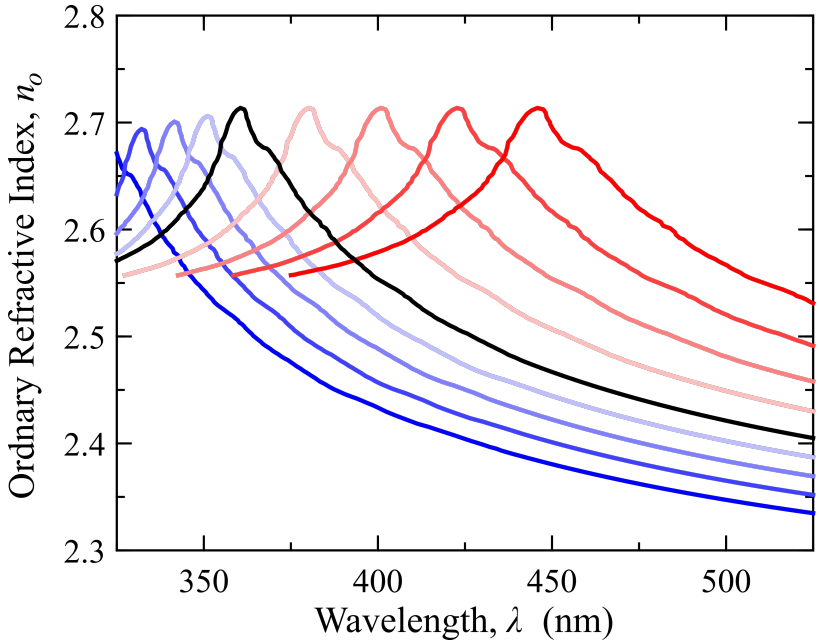

Figure A.2: (Ordinary) dispersion curve for GaN (black), $In_xGa_{1-x}N$ (red) and $Al_xGa_{1-x}N$ (blue). (Al_x,In_x) content increases from 5% - 20% in steps of 5% for each curve away from GaN.

$In_xGa_{1-x}N$ QWs — the refractive index of QWs is notoriously difficult to determine. [7, 8] A well-known result of the Kramer-Kronig relation is that the modified absorption (or gain) spectra changes the real refractive index from that of bulk $In_xGa_{1-x}N$. While there are theoretical treatments [9] that base the dielectric constant vs. wavelength on the In content and QW geometry, we assume the same index as bulk strained layers. In a waveguide with $In_xGa_{1-x}N$ waveguiding layers (refractive index larger than n_{eff}), this assumption will not greatly impact modal profiles since they are sufficiently thin compared to the mode and are close to the index of the waveguiding layers. However, in the absence of $In_xGa_{1-x}N$ waveguiding layers, the refractive index of the QWs becomes a critical parameter.

A.3 Optical absorption of (Al,In)GaN

The definition will use for absorption (or gain) is the coefficient of exponential decay (or growth) of the power of an electromagnetic (EM) wave. Since we only deal with non-magnetic materials, all power decay (or growth) occurs through interactions with the electric field. Thus, optical absorption (or gain) determines the imaginary part of the refractive index. In this work, we will choose to represent a "forward" propagating EM wave with the term $e^{i\omega t}$, so that absorption (or gain) is now represented by a positive (or negative) scalar value as the imaginary part of the refractive index.

Experimental measurements of $(Al_x,In_x)Ga_{1-x}N$ absorption have proven difficult. The limits of growth thickness and material quality have impeded simple bulk measurements. Specifically, the absorption spectra vs. alloy content and doping must be determined using thin grown layers. The thickness and material composition must be determined after growth through destructive analysis techniques like transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS). Any growth defects that arise, like those due to built-up strain of heteroepitaxy, will greatly skew the calculated absorption spectra. For this reason, many experiments to date only provide an order of magnitude of the absorption spectra.

Our procedure is to use the theoretical work of Kioupakis *et al.* [10] to model the shape of the absorption spectra vs. alloy content and doping. Their approach is to view all absorption as that of free-carrier like particles. These particles are the dopants in the material. Even in the case of Mg doping, a deep acceptor in GaN, the majority un-ionized state of Mg still acts as a recombination center, as determined through their computational first principles approach. Thus, all absorption is pro-

portional to the doping. This is an unintuitive conclusion: un-ionized states act as free-carriers, contributing to free-carrier absorption (FCA). We will see that this fact is an important driving factor in $(Al_x,In_x)Ga_{1-x}N$ waveguide design.

The absorption cross-section, σ, is what is determined by type of dopant (donor or acceptor/acceptor-like), type and concentration of alloy content (Al or In), as well as material quality (i.e. defect concentration). The absorption spectrum exhibits birefringence in the same manner as the real refractive index. It is important to recognize that all $(Al_x,In_x)Ga_{1-x}N$ material is doped in practice, with unintentional doping (UiD) providing more carriers than true intrinsic material would.

The 4^{th} order polynomial fits to the absorption cross-sections are provided by Kioupakis *et al.* Selecting the dopant type and EM field polarization allows one to calculate $\sigma(\lambda)$ due to phonons, alloy, and defects, with the latter two being a function of the specific material. These three values are then summed and multiplied by the doping concentration, denoted as ξ_A or ξ_D for acceptors or donors, respectively. However, we find that the quality of epitaxial growth is now good enough that the absorption cross-section is orders of magnitude less than that due to phonons and alloy content (though nothing can be said about ray scattering). The polynomial coefficients and required equations are re-printed below.

$$\alpha(x,\lambda) = \xi\left(\sigma_{\text{phonon}}(\lambda) + \sigma_{\text{alloy}}(x,\lambda)\right) \tag{A.11}$$

$$\alpha_{\text{phonon}}(\lambda) = 10^{18}\,\text{cm}^2 \times \sum_{i=0}^{4}\left(a_{\text{phonon},i}\right)\lambda^i \tag{A.12}$$

$$\alpha_{\text{alloy}}(x,\lambda) = 10^{18}\,\text{cm}^2 \times \frac{x(1-x)}{0.25(1-0.25)} \times \sum_{i=0}^{4}\left(a_{\text{alloy},i}\right)\lambda^i \tag{A.13}$$

The alloy assisted absorption cross-section was calculated using a 32-atom quasi-random structure of $In_xGa_{1-x}N$ ($x = 25\%$). We extend the use of this fit to the case of

Table A.4: Polynomial fit coefficients for determining phonon-assisted and alloy-assisted absorption cross-sections (from Kioupakis *et al.*).

	Ordinary: $\perp_c$		**Extraordinary:** $\parallel_c$	
Coefficients	ξ_A	ξ_D	ξ_A	ξ_D
phonons				
a0	-2.63E-01	5.55E+00	-2.86E+01	6.05E-01
a1 (nm^{-1})	2.00E-01	-5.63E-02	2.13E-01	-6.68E-03
a2 (nm^{-1})	-5.41E-04	2.04E-04	-5.67E-04	2.32E-05
a3 (nm^{-1})	6.29E-07	-3.06E-07	6.55E-07	-2.84E-08
a4 (nm^{-1})	-2.67E-10	1.79E-10	-2.76E-10	1.65E-11
alloy				
a0	-7.77E-01	-5.35E+01	1.75E+01	-4.85E+01
a1 (nm^{-1})	6.60E-01	4.50E-01	-1.18E-01	3.73E-01
a2 (nm^{-1})	-2.13E-03	-1.39E-03	2.51E-04	-1.06E-03
a3 (nm^{-1})	3.03E-06	1.88E-06	-1.61E-07	1.36E-06
a4 (nm^{-1})	-1.58E-09	-9.16E-10	0.00E+00	-6.40E-10

$Al_xGa_{1-x}N$, but recognize that it may deviate significantly. However, we know that the absorption cross-section of GaN is a lower bound. We also speculate that the equivalent In-content $In_xGa_{1-x}N$ is an upper bound, since the smaller-bandgap $In_xGa_{1-x}N$ will have more ionized dopants and free carriers for the same dopant concentration.

Finally, we used the above model to compare to total waveguide absorption (using the techniques described in this work) to the absorption found experimentally by Sizov *et al.* [11] and Melo *et al.* [12] To better match the experimental data, it was determined that a multiplicative factor of 2.3 should be use to scale the absorption

spectra shape.

A comparison of absorption spectra at a fixed doping concentration of $1 \times 10^{18}\,\mathrm{cm}^{-2}$ [Mg, Si] for $(Al_x,In_x)Ga_{1-x}N$ (0% - 30% alloy content, steps of 5%) is shown below.

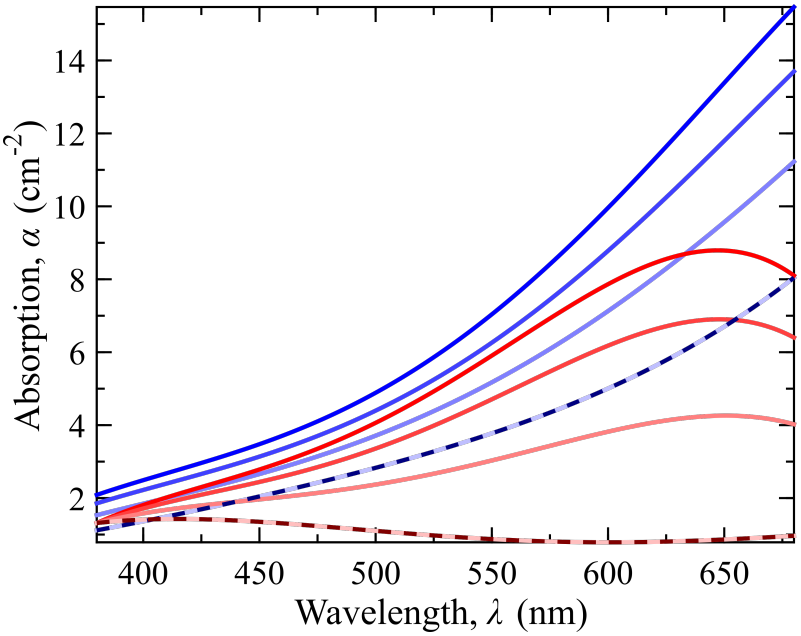

Figure A.3: (Ordinary) absorption spectra due to FCA for GaN (black dashed lines) and GaN alloys at a fixed doping concentration of $1 \times 10^{18}\,\mathrm{cm}^{-2}$ [Mg] (blue lines) and $1 \times 10^{18}\,\mathrm{cm}^{-2}$ [Si] (red lines). (Al_x,In_x) content increases from 10% - 30% in steps of 10% for each curve farther from that of GaN. This model is valid for $380\,\mathrm{nm} < \lambda < 680\,\mathrm{nm}$. Note that above-bandgap absorption is not included.

This model calculates the per-dopant absorption value to be higher for [Mg] than for [Si], and generally increase with longer wavelengths. The absorption of p-type $(Al_x,In_x)Ga_{1-x}N$ is exacerbated by the high [Mg] doping concentrations required: for an intended ionization level (in the absence of an internal electric field), approximately two orders of magnitude of doping is required. Thus, p-type $(Al_x,In_x)Ga_{1-x}N$ layers

will have a large material absorption compared to its n-type counterpart in the typical p-i-n junction of a GaN LD.

A.4 Optical constants of other materials

The optical constants for a large number of elemental and inorganic materials can be easily accessed online. [13] Selecting the material from a list, then selecting the appropriate (cited) source with the wavelength range of interest will give many of the optical constants required. For metals, this is most often a comma-separated list of wavelength vs. real and imaginary parts of the refractive index. For dielectrics or other non-absorbing materials, Sellmeier coefficients are most convenient.

Additionally, this work uses the organic material benzocyclobutene (BCB) as an electrically insulating optical cladding. The refractive index of BCB can be found on the manufacturer's website. [14] The absorption is assumed to be negligible around 450 nm and longer, [15] and was confirmed by ellipsometery at the Nanofabrication Facility at UCSB.

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Appendix B

Effective medium approximations

In practice, simulation of real waveguides often requires regions of the waveguide to be approximated as a single effective medium with a single dielectric constant, though it may be comprised of many materials and geometries. Depending on the nature of the volume to be simulated and the nature of the EM wave in question, we can simplify many geometries while still maintaining a high degree of accuracy in the simulation.

In all of the following effective medium approximations (EMAs), the following assumptions apply:

1. The size of geometries that comprise the volume to be approximated are sufficiently smaller than the optical wavelength (and mode profile) in the volume. [1]

2. The dispersion of the aggregates is inhomogeneous, i.e. distinct volumes or particles. [1]

3. The materials are non-magnetic.

4. The real parts of the complex refractive indices of the constituents are either both larger or both smaller than the imaginary parts [2] (e.g. both non-metal or both metal).

Furthermore, only volumes of two constituents are considered, but any of the EMAs can be extended to more than two.

It should be noted that first assumption is dependent on the electric field profile and its overlap with the effective medium in question. In general, a lower overlap with the effective medium will yield a more accurate approximation.

B.1 The Bruggeman approximation

Consider a material that is an aggregate of two distinct materials A and B (Fig. B.1) of fill fraction f_A and $(1 - f_A)$. If the shape of the constituent particles is random (i.e. randomly oriented with respect to the electric field), the dielectric constant ε_{eff} is given by solving Eq. B.1. [3]

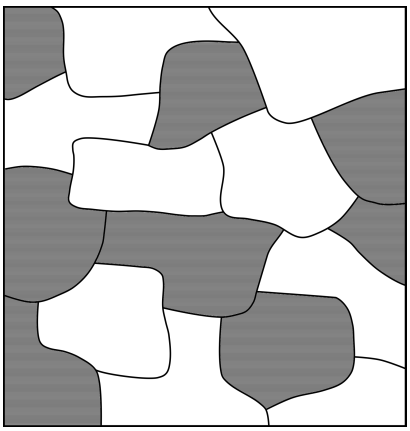

Figure B.1: Random particles of material A (shaded area) and material B.

$$f_A \frac{\varepsilon_A - \varepsilon_{\text{eff}}}{\varepsilon_A + 2\varepsilon_{\text{eff}}} + (1 - f_A) \frac{\varepsilon_B - \varepsilon_{\text{eff}}}{\varepsilon_B + 2\varepsilon_{\text{eff}}} = 0 \tag{B.1}$$

We can solve for ε_{eff} by finding the roots of the quadratic formula, choosing either the negative root for metal materials or the positive root for non-metals:

$$\begin{aligned} a =& -2 \\ b =& f_A(\varepsilon_A - 2\varepsilon_B) \\ &+ (1 - f_A)(\varepsilon_B - 2\varepsilon_A) \\ c =& \varepsilon_A \varepsilon_B \end{aligned} \tag{B.2}$$

This EMA gives reasonable values for all fill fractions, but will generally be more accurate ($< 5\%$ error) for particles of nominal radius ~ 2 orders of magnitude smaller than the free-space wavelength. Accuracy also increases for fill fractions that approach the extremes of 1 and 0.

B.2 The Maxwell Garnett approximation

A further simplified equation can be used for f_A approaching 0 or 1. [4] Qualitatively, this is the situation consisting of small particles of A dispersed in homogeneous media B:

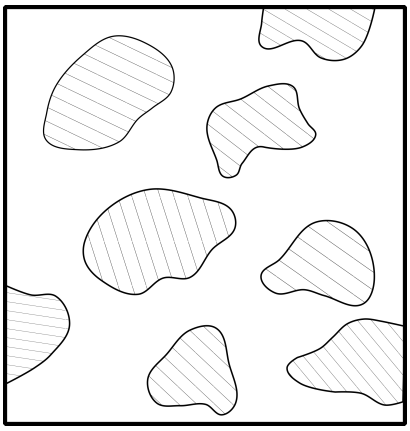

Figure B.2: Small and randomly oriented particles of material A (cross-hatched area) in matrix B.

$$\varepsilon_{\text{eff}} = \varepsilon_B \frac{\varepsilon_A + 2\varepsilon_B + 2f_A(\varepsilon_A - \varepsilon_B)}{\varepsilon_A + 2\varepsilon_B - f_A(\varepsilon_A - \varepsilon_B)} \tag{B.3}$$

As we deviate further from $f_A = 0$, this EMA will give a lower bound if $\varepsilon_A > \varepsilon_B$ and an upper bound if $\varepsilon_A < \varepsilon_B$. This can be seen in Fig. B.5.

B.3 The (rigorous bound) Bergman approximations

For the special case of a static electric field parallel or perpendicular on co-planar plates of material (Fig. B.3), the dielectric function is exactly solvable, regardless of fill fraction [5]:

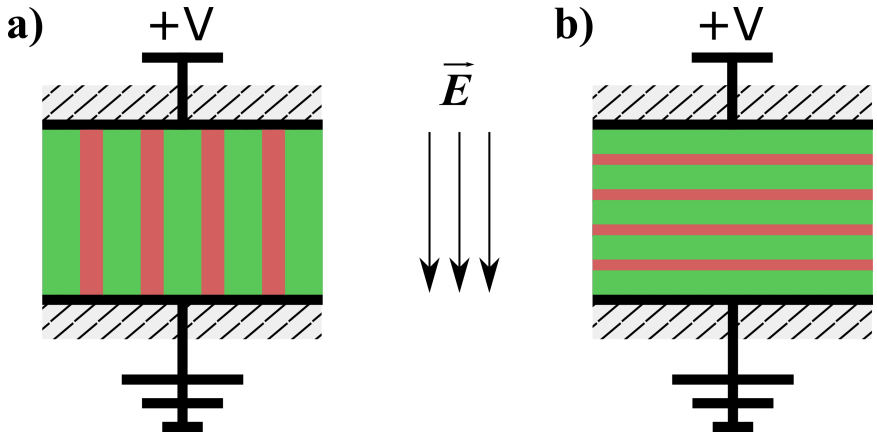

Figure B.3: Layers of material A (green) and B (red) with dielectric constants ε_A and ε_B, respectively, oriented **a)** parallel and **b)** perpendicular to the static electric field.

$$\text{TE:}\ \varepsilon_{\text{eff}} = f_A\left(\varepsilon_A\right) + \left(1 - f_A\right)\left(\varepsilon_B\right) \tag{B.4}$$

$$\text{TM:}\ {}^{1}\!/_{\varepsilon_{\text{eff}}} = f_A\left({}^{1}\!/_{\varepsilon_A}\right) + \left(1 - f_A\right)\left({}^{1}\!/_{\varepsilon_B}\right) \tag{B.5}$$

Intuitively, these formulae resemble the formulae for combining capacitors in parallel and in series, respectively. A TE- or TM-like guided mode is similar in that it consists of a nearly planar electric field, but this field happens to be oscillating. However, the general shape of the (electric) vector field is dependent on material dimensions, which is not the case in Fig. B.3 where the electric field is assumed to be infinite in the x- and z-dimension. Therefore, the following becomes a good approximation in the limit of small layer thicknesses compared to the optical wavelength.

Note that the selected case of polarization is in regards to the patterned feature: for TE, the oscillating electric field is parallel to the planes of material while for TM, the oscillating electric field is perpendicular to said planes. Therefore, depending on the slab orientation, a common TE^z mode will be TE- or TM-like (Fig. B.4) for the purposes of using Eq. B.4.

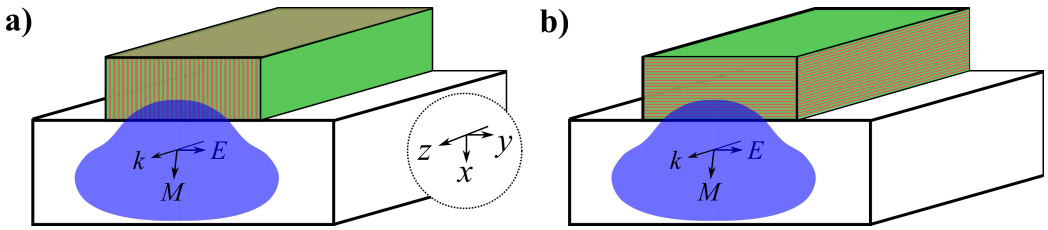

Figure B.4: Orientation of the electric field of (a) a TE-like and (b) a TM-like electromagnetic wave (blue 2-D mode profile) in a waveguide *with respect to* a 1-D patterned layer on top. Note that the optical mode is TE^z in both cases.

B.4 Comparison of EMAs

As a simple comparison, Fig. B.5 shows the approximated refractive index, n_{eff} ($= \sqrt{\varepsilon_{\text{eff}}}$), vs. fill fraction, f_A, for two materials, A: air ($n = 1$) and B: GaN ($n = 2.46$):

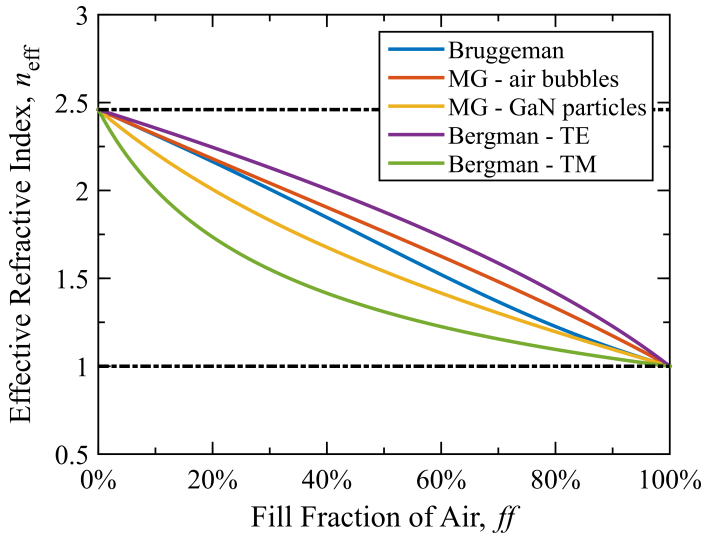

Figure B.5: Effective medium approximations for a heterogeneous mix of two distinct materials. Each curve represents an approximation using specific assumptions, as listed above.

Note that the Maxwell Garnett EMA provides upper and lower bounds for n_{eff}

when considering irregularly shaped materials (i.e. random orientations and shapes). The Bruggeman EMA exhibits more extreme values for n_{eff} because of the non-random shape compared to the electric field.

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Appendix C

MATLAB code excerpts — TMM

A good introduction to the formalism of the Transfer Matrix Method is described in chapter 5 of *Confined Photon Systems* by V. Savona, [1] as well as in Appx. A of *Embedded Photonic Crystals for High-Efficiency GaN-based Optoelectronic Devices* by Elison Matioli. [2] The goal of this method is to reduce a layered stack of materials into a single matrix that represents the "transfer" of an electromagnetic (EM) wave from one side of the stack to the other.

The square matrix represents a linear system describing the change in a forward propagating wave and a backward propagating wave traveling perpendicular to a 1-D system (Fig. 2.1). Thus, each transfer matrix has dimensions 2×2, and can be directly multiplied together to find the transfer matrix of a combined system. When we assume all non-magnetic materials, we can fully describe the system with a 2-element basis vector of the electric field: one traveling "up" in the negative y-direction, and one traveling "down", which together form the standing wave in the shape of a mode.

This method is very similar to the well-known transmission matrix and scattering matrix formalisms. The difference is that the formulation of the transfer matrix allows chain left-hand-side multiplication to represent a system, as we will see below.

This appendix will provide a brief summary of the mathematical formalism of TMM for both TE^z and TM^z, then describe a computational approach using the matrix-based MATLAB (MATrix LABoratory) coding language. The code has been highly optimized for speed, dealing with equations in a matrix-oriented fashion instead of the more intuitive sequential "for-loop" approach. Solutions to the linear system are found using a numerical brute force approach — an array of trial solutions is used as the input and simultaneously validated. The gains in computational speed come at the cost of memory resources, which should be judiciously allocated. While a basic knowledge of MATLAB code and syntax is assumed, specialized functions and procedures are explicitly defined.

C.1 The TMM formalism

We start with the matrix M that satisfies the transfer of the electric field from position 1 to position 2:

$$\begin{bmatrix} \boldsymbol{E}^{\boldsymbol{up}}{}_2 \\ \boldsymbol{E}^{\boldsymbol{dn}}{}_2 \end{bmatrix} = \begin{bmatrix} \boldsymbol{M}_{(1,1)} & \boldsymbol{M}_{(1,2)} \\ \boldsymbol{M}_{(2,1)} & \boldsymbol{M}_{(2,2)} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{E}^{\boldsymbol{up}}{}_1 \\ \boldsymbol{E}^{\boldsymbol{dn}}{}_1 \end{bmatrix} = \boldsymbol{M}^{1:2} \cdot \begin{bmatrix} \boldsymbol{E}^{\boldsymbol{up}}{}_1 \\ \boldsymbol{E}^{\boldsymbol{dn}}{}_1 \end{bmatrix} \tag{C.1}$$

Therefore, if we want to find out the electric field at position 3, passing through position 2 and starting from position 1:

$$\begin{bmatrix} \boldsymbol{E}^{\boldsymbol{up}}{}_3 \\ \boldsymbol{E}^{\boldsymbol{dn}}{}_3 \end{bmatrix} = \boldsymbol{M}^{2:3} \cdot \boldsymbol{M}^{1:2} \cdot \begin{bmatrix} \boldsymbol{E}^{\boldsymbol{up}}{}_1 \\ \boldsymbol{E}^{\boldsymbol{dn}}{}_1 \end{bmatrix} = \boldsymbol{M}^{1:3} \cdot \begin{bmatrix} \boldsymbol{E}^{\boldsymbol{up}}{}_1 \\ \boldsymbol{E}^{\boldsymbol{dn}}{}_1 \end{bmatrix} \tag{C.2}$$

In this fashion, we can find the value of the electric field at the final position given the value of the initial position and all of the transfer matrices in between. With this formalism and wording, it is implied that the initial position, and therefore the initial layer, is at the "bottom" of the stack, and that the final position is at the top. We do this so that the resulting electric field profile is measured as "depth from the surface". Therefore, the labels of "up" and "dn" reflect the positive and negative y-directions respectively.

A guided mode is a special case of the transfer matrix. In the core of the waveguide, there exists a large electric field, while outside the waveguide is only an evanescent tail of small magnitude. Therefore, we expect the indication of a mode to be that input field at one side of a stack of N layers results in minimal field at the other, or:

$$\begin{bmatrix} \sim 0 \\ \boldsymbol{E^{dn}}_{top} \end{bmatrix} = \begin{bmatrix} \boldsymbol{M^{1:N}}_{(1,1)} & \boldsymbol{M^{1:N}}_{(1,2)} \\ \boldsymbol{M^{1:N}}_{(2,1)} & \boldsymbol{M^{1:N}}_{(2,2)} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{E^{up}}_{bot} \\ 0 \end{bmatrix} \tag{C.3}$$

$$\begin{bmatrix} \boldsymbol{E^{up}}_{top} \\ \sim 0 \end{bmatrix} = \begin{bmatrix} \boldsymbol{M^{1:N}}_{(1,1)} & \boldsymbol{M^{1:N}}_{(1,2)} \\ \boldsymbol{M^{1:N}}_{(2,1)} & \boldsymbol{M^{1:N}}_{(2,2)} \end{bmatrix} \cdot \begin{bmatrix} 0 \\ \boldsymbol{E^{up}}_{bot} \end{bmatrix} \tag{C.4}$$

For these two conditions to be met, the following relations hold:

$$\left|\boldsymbol{M^{1:N}}_{(1,1)}\right| \cong 0 \tag{C.5}$$

$$\left|\boldsymbol{M^{1:N}}_{(2,2)}\right| \cong 0 \tag{C.6}$$

In practice, we search for coinciding local minimum values of $\left|\boldsymbol{M^{1:N}}_{(1,1)}\right|$ and $\left|\boldsymbol{M^{1:N}}_{(2,2)}\right|$. Furthermore, for a well-behaved waveguide, both conditions will always be met simultaneously.

This technique gives us insight into what structures may be computationally taxing. For instance, if the cladding layers on one side of the waveguide are too thick, the magnitude of the evanescent field will become too small for double-floating point precision, effectively becoming zero for all trial $\tilde{n}_{\text{eff}}$. Then the matrix element minimums and modes will not be found.

C.2 The propagation transfer matrix

When we reduce each layer into matrices representing the propagation of an electric field through a uniform material, we find:

$$\boldsymbol{M}_{prop} = \begin{bmatrix} e^{i\,k_y\,t} & 0 \\ 0 & e^{-i\,k_y\,t} \end{bmatrix} \tag{C.7}$$

where k_y is the vertical component of the wavevector in the layer and t is the thickness of the layer. For computational ease, we can rewrite this as:

$$\boldsymbol{M}_{prop} = \begin{bmatrix} up & 0 \\ 0 & dn \end{bmatrix}, \quad up = e^{i\,k_y\,t}, \quad dn = {}^{1}\!/_{up} \tag{C.8}$$

where up represents the positive y-direction propagation of electric field and dn the reverse. In looking for a mode (standing wave) in the xy-plane that is a traveling in the z-direction, we know that the components of the wavevector in each layer are:

$$k_z^2 = k_x^2 + k_y^2, \quad k_z = \frac{2\,\pi\,\tilde{n}_{\text{eff}}}{\lambda_o}, \quad k_x = \frac{2\,\pi\,\tilde{n}}{\lambda_o} \tag{C.9}$$

where λ_o is the chosen free-space wavelength, $\tilde{n}$ is the complex refractive index of the material, and $\tilde{n}_{\text{eff}}$ is the effective complex refractive index of the mode. This propagation matrix formulation holds for both TE^z and TM^z modes.

Determining the value of $\tilde{n}_{\text{eff}}$ is the main goal of the simulation. Therefore, when we input an array of trial $\tilde{n}_{\text{eff}}$, we can form the corresponding wavevector components and propagation matrix. Now, we can create the corresponding MATLAB function:

```
function propMat = PropagationMatrices(kt,tList)
% find the propagation matrices for a list of layers of thickness
% t, using the array of trial transverse wavevectors, kt
    % get output dimensions
    [nLayers, nModes] = size(kt);

    % create elements for layer interface matrices
    up = exp(1i*bsxfun(@times,kt,tList));
    up = up.';
    up = reshape(up,[1,1,numel(up)]);
    dn = 1./up;

    % construct output
    propMat = [up,zeros(1,1,nLayers*nModes);
    zeros(1,1,nLayers*nModes),dn];
    propMat = reshape(propMat,2,2,nModes,nLayers);
end
```

The first input of this function is `kt`, the transverse wavevector, known to us as k_y. This variable is a two-dimensional matrix, with the first dimension representing the individual layers of the stack and the second representing the trials of $\tilde{n}_{\text{eff}}$. It can be a large matrix — if there are 100 layers and 128 trials, then the matrix will be 51,200 elements. The second input, `tList`, is an array of the layer thicknesses and should match the first dimension of `kt`.

The function `bsxfun` allows quick element-by-element computation of two matrices using implicit expansion. Therefore, the input `tList` is expanded along its singleton second dimension (repeating the original array) to match the size of `kt` before each corresponding element is multiplied together.

The function `reshape` changes the perceived shape of the matrices. The elements of the matrix do not actually move in memory, so it is an extremely fast procedure. By creatively constructing the elements of Eq. C.3, the final output can be created with a minimal amount of computational resources.

The output of the function is the expanded matrix representation of Eq. C.3. It is a 4-D matrix, with the first two dimensions representing the 2×2 transfer matrix, the 3rd dimension representing the different trials, and the 4th representing the layers of the waveguide.

C.3 The interface transfer matrix

We define the matrix describing the transfer of the TE^z-polarized EM wave through the yz-plane interface of material 1 and material 2 by:

$$\boldsymbol{M}^{\mathbf{1:2}}{}_{inter} = \begin{bmatrix} \dfrac{(k_2)_y + (k_1)_y}{2\ (k_2)_y} & \dfrac{(k_2)_y - (k_1)_y}{2\ (k_2)_y} \\ \\ \dfrac{(k_2)_y - (k_1)_y}{2\ (k_2)_y} & \dfrac{(k_2)_y + (k_1)_y}{2\ (k_2)_y} \end{bmatrix} \tag{C.10}$$

For computational ease, we can write the above as:

$$\boldsymbol{M}^{\mathbf{1:2}}{}_{inter} = \frac{1}{2}\left(1 + \begin{bmatrix} k_r & -k_r \\ -k_r & k_r \end{bmatrix}\right), \quad k_r = \frac{(k_1)_y}{(k_2)_y} \tag{C.11}$$

For TM modes, we have a slightly different interfacial transfer matrix:

$$\boldsymbol{M}^{\mathbf{1:2}}{}_{inter} = \begin{bmatrix} \dfrac{(n_1)^2\,(k_2)_y + (n_2)^2\,(k_1)_y}{2\,(n_1)^2\,(n_2)^2\,(k_2)_y} & \dfrac{(n_1)^2\,(k_2)_y - (n_2)^2\,(k_1)_y}{2\,(n_1)^2\,(n_2)^2\,(k_2)_y} \\ \\ \dfrac{(n_1)^2\,(k_2)_y - (n_2)^2\,(k_1)_y}{2\,(n_1)^2\,(n_2)^2\,(k_2)_y} & \dfrac{(n_1)^2\,(k_2)_y + (n_2)^2\,(k_1)_y}{2\,(n_1)^2\,(n_2)^2\,(k_2)_y} \end{bmatrix} \tag{C.12}$$

Again, we simplify the equation:

$$\boldsymbol{M}^{\mathbf{1:2}}{}_{inter} = \frac{1}{2}\left(n_r + \begin{bmatrix} \rho & -\rho \\ -\rho & \rho \end{bmatrix} \right), \quad n_r = \frac{n_1}{n_2}, \quad \rho = \frac{k_r}{n_r} \tag{C.13}$$

The corresponding MATLAB function is:

```
function interMat = InterfaceMatrices(kt,nkList,TEFlag)
% find the interfacial matrices for a list of layers with complex
% refractive indices nk, using the array of trial transverse wave
% vectors, kt. The TE mode is found by default, but can be switched
% to TM by setting TEFlag to false.

    % check optional input and get output dimensions
    if ¬exist('TEFlag','var'), TEFlag = true; end
    [nLayers,nTrialNEff] = size(kt);

    % create elements for layer interface matrices
    kt_ratio = (kt(1:end-1,:)./kt(2:end,:)).';
    if TEFlag, n_ratio = 1;
    else n_ratio = (nkList(1:end-1)./nkList(2:end)).';
    end

```

```
17      % construct output
18      interMat = kt_ratio./n_ratio;
19      interMat = reshape(interMat,[1,1,size(interMat)]);
20      n_ratio = reshape(n_ratio,[1,1,size(n_ratio)]);
21      interMat = [ interMat, -interMat
22                  -interMat,  interMat];
23      interMat = bsxfun(@plus,n_ratio,interMat);
24      interMat = interMat./2;
25      interMat = reshape(interMat,2,2,nTrialNEff,nLayers-1);
26  end
```

The input `kt` is the same as the last function; it is a rather large 2-D matrix. The input `nkList` is an array of the complex refractive index of each layer. It is only needed if the TM^z mode is requested instead of the usual TE^z.

Initially, the inputs are used to compute the reduced variables `kr` and `nr`. Then, the interface matrix is constructed in a similar manner to the propagation matrix, albeit with more mathematical operations. It has almost the same size as the 4-D propagation matrix output, but one less 2×2 matrix as there is one less interface than layers to propagate through. This difference will have to be accounted for when the matrices are multiplied together.

C.4 The combined transfer matrix

Given an array of $\boldsymbol{M}_{prop}$ and an array of $\boldsymbol{M}_{inter}$, we must multiply each $\boldsymbol{M}_{prop}$ of a layer with the $\boldsymbol{M}_{inter}$ of the adjacent layer. Then, the array containing these transfer matrices must be multiplied together in the correct order. This is accomplished by the following:

```
function mMat = TransferMatrices(kt,tList,nkList,TEFlag)
% get the final transfer matrix of the stack for all trial nk's
    % check optional input
    if ¬exist('TEFlag','var'), TEFlag = true; end

    INTER = ModeSolver.InterfaceMatrices(kt,nkList,TEFlag);
    PROP = ModeSolver.PropagationMatrices(kt,tList);
    PROP = PROP(:,:,:,1:end-1);
    LAYERS = multiprod(INTER,PROP);
    LAYERS = permute(LAYERS,[1,2,4,3]);
    mMat = mprod(LAYERS,'reverse');
end
```

The above function leverages the previously defined functions to create the arrays of $\boldsymbol{M}_{prop}$ and $\boldsymbol{M}_{inter}$. Then, the last matrix of $\boldsymbol{M}_{prop}$ is removed. This done so that the sizes of $\boldsymbol{M}_{prop}$ and $\boldsymbol{M}_{inter}$ match. If we make sure to pad the layer stack with zero-thickness air on top and bottom, then removing this 2×2 matrix will just be removing an the identity matrix. Since the following steps are matrix multiplications, the end result will not be affected. To multiply the two arrays of transfer matrices, the function `multiprod` [3] is used. This freely available function efficiently multiplies two multi-dimensional arrays by their matching non-singleton dimension. It is a great alternative to using a for-loop, which would exponentially increase computing time. However, after creating the single array of transfer matrices called `LAYERS`, we still need to chain multiply the $\boldsymbol{M}^{[\boldsymbol{LAYERS}]}$ together. For this, we use the function `mprod`:

```
function sqMats = mprod(M,reverse)
    % Multiply *many* square matrices together, stored along 3rd ...
```

```
        axis.
    % Extra dims are conserved; use 'permute' to change axes of "M".
    % Speed gained by recursive use of 'multiprod' (Leva, 2010).

    if ¬exist('reverse','var') || isempty(reverse), reverse = false;
    elseif strcmp(reverse,'reverse'), reverse = true; end
    assert(isa(reverse,'logical'),..
        'Second input must be "reverse" or a logical')

    % save extra dimensions, then reshape
    dims = size(M);
    M = reshape(M,dims(1),dims(2),dims(3),[]);

    % Check if M consists of multiple matrices...
    % split into two sets and multiply using multiprod repeatedly
    siz = size(M,3);
    extra = [];
    while siz > 1 || ¬isempty(extra)
        % check for odd number of matrices
        if mod(siz,2)
            if isempty(extra), extra = M(:,:,end,:);
            else M = cat(3,M,extra); extra =[];
            end
        end

        % create two smaller 3D arrays
        X = M(:,:,1:2:end-1,:); % odd pages
        Y = M(:,:,2:2:end,:); % even pages

        % actual matrix multiplication
```

```
32          if reverse, M = multiprod(Y,X);
33          else M = multiprod(X,Y); end
34          siz = size(M,3);
35      end
36
37      % reshape to original dimensions, minus the third axis.
38      dims(3) = [];
39      sqMats = reshape(M,dims);
40  end
```

Rather than multiplying each 2×2 matrix sequentially, this function iteratively breaks the array of matrices in half and uses the multiprod function to combine them. It is still an iterative process, but cuts the computation time by $\sim \log_2(N)$. It also allows for multiplication in the reverse direction, satisfying the right-hand side multiplication requirement.

C.5 Finding the guided modes

Using the above functions, we can input an array of trial $\tilde{n}_{\text{eff}}$ into the given stack and return an array of transfer matrices $\boldsymbol{M}^{\mathbf{1:N}}$. We choose our array by making an educated guess as to the bounding limits of the modes. A good guess is that the $\tilde{n}_{\text{eff}}$ must be between the refractive index of the cladding and waveguiding layers. The imaginary part must also be set. It should lie between that of the least absorbing layer and the most absorbing core element (e.g. waveguiding layer or quantum well). We then choose the linearly spaced grid based on these limits and the number of trials we would like to test.

By checking the elements of $\boldsymbol{M}^{\mathbf{1:N}}$, we can find the cases of minimal electric field

transmission. However, we must account for the fact that we are looking for local minimums on the 2-D complex plane.

```
% get the (1,1) and (2,2) elements of the 2X2 transfer matrix
mMat = obj.TransferMatrices(kt,tList,nkList,obj.TEFlag);
recieve = abs(mMat(1,1,:));
transmit = abs(mMat(2,2,:));
txrx = transmit + recieve;
txrx = reshape(txrx(:),[nNr,nNi,nModes]);
neff = reshape(neff,[nNr,nNi,nModes]);

% find modes from minimum transmission vs. neff's
if complexFlag, minDist = [1,1];
else minDist = [1,0]; end
[¬,minMap,¬] = localMin(txrx,minDist,1,1);
modes = neff(minMap);
```

The first half of the above code excerpt uses all previous code to create an array of matrix elements vs. trial $\tilde{n}_{\text{eff}}$. The second half of the above excerpt deals with the search for the local minima on the complex plane using an in-house function called `localMin`. The output `minMap` returns a logical index array of the same size as the input indicating the local minima. With the minima found, the corresponding $\tilde{n}_{\text{eff}}$ will be those of valid guided modes.

With a single array of trial $\tilde{n}_{\text{eff}}$, the precision with which we found the mode may not be sufficient. Since inputting a large array becomes intractable, we can instead refine our initial bounds to the values immediately surrounding each local minimum, then re-run the mode finding procedure. Depending on the waveguide, choice in bounding limits, and size of the trial array, sufficiently precise modes can usually be

determined in a handful iterations.

C.6 Finding the electric field profile

Once the modes are found, we can find the value of the electric field profile at each slice of waveguide, given a small input at one side. The computational procedure is similar to that of finding the modes. Instead of many trials of $\tilde{n}_{\text{eff}}$, only the $\tilde{n}_{\text{eff}}$ of the modes are used. However, each layer of the stack must now be discretized into many slices for adequate resolution of the profile. In the code below, the number of layer slices is provided as the variable `obj.nLSlices`; we fix it at 128 to limit computational resource usage:

```
% Break up layers into small slices
nSlices=obj.nLSlices*nLayers;
lSliceTs = 1/obj.nLSlices*tList; % layer-slice thicknesses
slicing = 1/obj.nLSlices/2:1/obj.nLSlices:1; % linear spacing
slicing = bsxfun(@times,slicing.',tList.');

% create kt matrix of size [nLayers,nModes]
k_o=2*pi/wg.wl; % freespace wavenumber
kList=nkList*k_o; % phase wavenumbers for each layer
beta=neff*k_o; % group wavenumbers for each mode
kt = sqrt(bsxfun(@minus,kList.^2,(beta.^2).')); % transverse k
% no meta-materials, so real component of kt is always positive
kt(real(kt)<0) = -kt(real(kt)<0);

% create layer interface matrices
INTER = ModeSolver.InterfaceMatrices(kt,nkList);
```

```
17
18 % create propagation matrices
19 % ... half slice propagation first
20 PROP_2 = ModeSolver.PropagationMatrices(kt,lSliceTs./2);
21 % mutliply layers and half-slice propagations
22 PROP_2 = PROP_2(:,:,:,1:end-1);
23 LAYERS = multiprod(INTER,PROP_2);
24
25 % kt for each layer slice FROM its layer interface
26 kt = permute(kt,[3 1 2]);
27 kt = repmat(kt,[obj.nLSlices 1 1]);
28 kt = reshape(kt, nSlices, nModes);
29 PROP = ModeSolver.PropagationMatrices(kt,slicing(:));
30 PROP = reshape(PROP,2,2,nModes,obj.nLSlices,nLayers);
```

Breaking each layer into an equal number of slices is the easiest matrix approach. It has the advantage that small important layers like QWs will have the appropriate resolution. Unfortunately, if there are many small layers, the computational time will be greatly increased (we set the upper limit to be 750 defined layers). This is because the field in each layer of the stack must be found in sequential order, propagating the input electric field from one side of the stack to the other:

```
1 % initialize wave and pass wave through layer interface
2 wave=zeros(2,1,nModes,obj.nLSlices,nLayers);
3 % small amount entering bottom of structure, nothing exiting
4 wave_init = [ones(1,1,nModes,obj.nLSlices);
5              zeros(1,1,nModes,obj.nLSlices)];
6 for l = 1:(nLayers-1)
7     % propagate wave in current layer
```

```
8       wave(:,:,:,:,l) = multiprod(PROP(:,:,:,:,l),wave_init);
9       % propagate wave of last slice through layer interface
10      wave_init = multiprod(LAYERS(:,:,:,l),...
11                  wave(:,:,:,obj.nLSlices,l));
12      % reshape initial layer wave for all slices
13      if nModes==1
14          d = wave_init(1); u = wave_init(2);
15          wave_init = [d*ones(1,1,1,obj.nLSlices);
16                       u*ones(1,1,1,obj.nLSlices)];
17      else
18          wave_init = repmat(wave_init, [1 1 1 obj.nLSlices]);
19      end
20  end
21  wave = wave(:,:,:,:,2:end-1);
22  wave = reshape(permute(wave,[4 5 3 2 1]),...
23                 nSlices-2*obj.nLSlices,nModes,2);
24
25  waveDn = wave(:,:,1);
26  waveUp = wave(:,:,2);
```

The final two lines of the above code excerpt give the electric field profiles of the upward traveling wave and the downward traveling wave. The addition of these two fields gives the standing-wave profile that is the guided mode.

References

[1] V. Savona, "Linear Optical Properties of Semiconductor Microcavities with Embedded Quantum Wells," in *Confined Photon Systems* (H. Benisty, C. Weisbuch, É. Polytechnique, J.-M. Gérard, R. Houdré, and J. Rarity, eds.), vol. 531 of *Lecture Notes in Physics*, ch. Linear Opt, pp. 173–182, Springer Berlin Heidelberg, 1999.

[2] E. d. N. Matioli, *Embedded photonic crystals for high-efficiency gallium nitride-based optoelectronic devices*. PhD thesis, University of California, Santa Barbara, 2010.

[3] P. de Leva, "MULTIPROD," 2010.

Appendix D

Process travelers

In §D.1, the process traveler snippet of the holography process used in the AGC-LD (1st generation) is given. In §D.2 the full process traveler for the EGC-LD device (2nd generation) is given. The EGC-LD was fabricated using an electron beam lithography process instead of holography.

The travelers are organized by major process step, usually one per page. For step, the procedure, up to three parameters (***P1***, ***P2***, ***P3***), and up to two process times (***T1***, ***T2***) are given. Notes and setup time (***T0***) are also provided. Finally, the total times for each sub-step and major process step are calculated.

D.1 Process traveler: holography

A snippet of the holography process used in the AGC-LD (1st generation) device. Note that the SiN_x layer acts as both the anti-reflection coating for the holography and the hard mask for the subsequent GaN dry etch (provided in *Appx. D.2*).

Hard Mask Deposition - 3:24

Equipment	*ID #*	*Procedure*	*P1*	*P2*	*P3*	*T1*	*T2*	*Notes*	*T0*
Pre-Clean - 0:54									
PECVD	26	Run clean: _30CLNSIN				0:30:00	0:02:00		0:10:00
Solvent Bench	27	Clean, sonicate on high	Acetone	IPA		0:02:00	0:02:00		0:01:00
	28	Rinse & dry	DI	N2		0:01:00	0:01:00		0:01:00
HF Bench	29	Native oxide strip: Si Mon #1	BHF	DI		0:02:00	0:01:00		0:01:00
SiNx Deposition - 2:30									
PECVD	30	Load Si Mon #1 and sample							0:02:00
	31	Run 15nm SiN dep: "_SIN15.PRC"				0:02:00			0:05:00
	32	Clean an Al cup	Acetone	IPA	DI			To remove machining oil	0:02:00
	33	Unload, water dip, dry; in clean Al cup	DI	N2		0:01:00	0:01:00	Si Mon #1 and sample; to terminate pinholes	0:01:00
	34	Run 15nm SiN dep: "_SIN15.PRC"				0:02:00			0:05:00
	35	Unload, water dip, dry; in clean Al cup	DI	N2		0:01:00	0:01:00	Si Mon #1 and sample; to terminate pinholes	0:01:00
	36	Copy "_SIN10.PRC" to "nedy_jSIN.PRC"							0:01:00
	37	Load Si Mon #1 and sample							0:05:00
	38	Edit target thickness of "nedy_jSIN.prc"	48 nm					set to half intended thickness	0:05:00
	39	~48nm SiNx Dep: "nedy_jSIN.PRC"				0:10:00			0:15:00
	40	Unload, water dip, dry; in clean Al cup	DI	N2		0:01:00	0:01:00	Si Mon #1 and sample; to terminate pinholes	0:01:00

Ellipsometer (JAW)	41	Measure Si Mon #1: "Standard"	55°	85°	10°	0:05:00			0:03:00
	42	Analysis: "Nedy/SiNx on Si.mod"	250nm	650nm				Record thickness and index @ {325nm, 632.8nm}	0:02:00
PECVD	43	Calc.: "Grating Calculator.xlsx: SiNx Dep"						Use calc to find remaining thickness setpoint based on thickness and index of Si Monitor #1b	0:02:00
	44	Edit nedy_jSIN.PRC thickness	25 nm					use value found in grating calculator	0:02:00
	45	Load Si Mon #1 and sample							0:02:00
	46	~25nm SiNx Dep: "nedy_jSIN.PRC"				0:05:00			0:15:00
Ellipsometer (JAW)	47	Measure Si Mon #1: "Standard"	55°	85°	10°	0:05:00			0:03:00
	48	Analysis: "Nedy/SiNx on Si.mod"	250nm	650nm				Record thickness and index @ {325nm, 632.8nm}	0:02:00
PECVD	49	Repeat steps [33-48] if necessary						only if thickness < Grating Calc. - 3nm	0:36:00
Microscope	50	Inspect							0:05:00

PhC Holography - 1:59

Equipment	*ID #*	*Procedure*	*P1*	*P2*	*P3*	*T1*	*T2*	*Notes*	*T0*

Laser Warm-Up - 1:01

PL/HL	46	Warm up He-Cd laser				1:00:00			0:01:00

Pre-Clean - 0:08

Solvent Bench	47	Sonicate on low	Acetone	Methanol		0:02:00	0:02:00		0:01:00
	48	Rinse & dry	DI	N2		0:01:00	0:01:00		0:01:00

PR Spin - 0:21									
PR Bench	49	Dehydration bake; let cool	115C			0:10:00	0:01:00		0:01:00
	50	Mount on blue tape						mount dummies of same thickness adjacent	0:02:00
	51	Adsorb; spin wetting agent	HMDS	3 krpm	10 krpm/s	0:00:20	0:00:30	Dispense using filter. Makes PR less fragile	0:01:00
	52	Spin PR: ~235nm thick	TSMR-iN027 pm	3 krpm	10 krpm/s	0:00:30		Dispense using filter. Negative PR for wider lines (150 nm lines/150 nm gaps)	0:01:00
	53	Unmount; clean backside	EBR100					scrape corners with razor blade	0:02:00
	54	Soft bake	90 °C			0:01:30			0:01:00

Holography - 0:20									
PL/HL	55	Calibrate He-Cd laser, H&V	8/13/18 mm	11 mm				Record powers; use L@(13, 11) below	0:10:00
	56	Expose: T~300 nm, D~55%	120 mJ	30°		*0:05:00*		T1 calc.: P1/L; {40.5°|30°} for {250|300} nm pitch	0:05:00

PR Develop - 0:09									
Develop Bench	66	Develop; rinse	AZ300MIF	DI		0:02:00	0:01:00	Very little agitation; use forceps	0:01:00
Microscope	67	Inspect lithography							0:05:00

PhC Etch - 3:42

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
PR Descum - 0:04									
PEII	68	PR Descum: 20 nm	300mT	100W		0:00:20		VERY IMPORTANT	0:04:00
SiNx Dry Etch - 1:04									
ICP #2	69	Gas change: *SF_6 -> CF_4 , Ar -> CHF_3*				0:05:00		if necessary	0:03:00
	70	Etch test recipes: *109, 102*				0:04:00	0:04:00	if necessary	0:03:00
	71	Clean & load O_2 cleaning wafer	Acetone	IPA	DI/N2			Clean & Check backside especially	0:05:00
	72	O_2 clean, Recipe: 103	40 sccm	900/100 W	5.0Pa	0:10:00			0:02:00
	73	Clean & load seasoning wafer	Acetone	IPA	DI/N2			Clean & Check backside especially	0:05:00
	74	CF_4/CHF_3 coat, Recipe: 126	30/10 sccm	900/50 W	0.5Pa	0:01:10		Check recipe, it's changed often	0:02:00
	75	Clean & load etch carrier wafer w/sample	Acetone	IPA	DI/N2			Mount w/a little Santovac diffusion pump oil	0:05:00
	76	**110nm** CF_4/CHF_3 **etch**, Recipe: 126	30/10 sccm	900/50 W	0.5Pa	0:00:45			0:02:00
	77	Load O_2 cleaning wafer (C2)							0:01:00
	78	O_2 clean, Recipe: 103	40 sccm	900/100 W	5.0Pa	0:05:00			0:02:00
	79	Unload carrier, unmount sample	Acetone	IPA	DI			careful not to scratch sample, PhC are fragile	0:05:00

Pre-Clean - 0:06									
Solvent Bench	80	Clean, agitate w/pipette	Acetone	IPA		0:01:00	0:01:00		0:01:00
	81	Rinse & dry	DI	N_2		0:01:00	0:01:00		0:01:00

PR Ash - 0:10									
GaSonics	82	Recipe: #7; run twice	350°			0:02:00	0:02:00	temperature maintained for ~2 min each run	0:06:00

GaN Dry Etch - 2:17									
Uniaxis Etch	83	Clean & load Si cleaning wafer	Acetone	IPA	DI/N2			Clean & Check backside especially	0:05:00
	84	"O2-clean 60min-200C"	50 sccm	800/200 W	10mTorr	1:00:00		cleans chamber	0:10:00
	85	Load Sapphire carrier w/2" GaN dummy							0:05:00
	86	BCl_3 & Cl_2/Ar Season: "Nedy PhC GaN Season-200C"	50 sccm 7/7 sccm	500/50 W 200/5 W	10mTorr 2mTorr	0:00:40	0:15:00		0:15:00
	87	Load Ni carrier wafer w/dummy&sample						Use same 2" GaN dummy from season	0:05:00
	88	**275nm** BCl_3 & Cl_2/Ar **Etch**: "Nedy PhC GaN Etch-200C"	50 sccm 7/7 sccm	500/50 W 200/5 W	10mTorr 2mTorr	0:00:40	0:05:50	50/50 PhC etch rate: 50nm/min + 10nm Planar etch rate: ~26.5nm/min + 30nm	0:15:00

D.2 Process traveler: EGC-LD

The full process traveler for the EGC-LD (2^{nd} generation) device. The traveler starts with an optional epitaxial characterization, then details a full GaN-to-Si bonding process before the actual EGC-LD process.

Polished Facet, Etched Gap LD Process **v3.0** **Last revised: 3/28/16**

Author: J. Nedy **Confidential**

Reference: Etched Facet PhC LD Process V2 **Total Time: 117:50:30**

[Si Sub-mount] Seed Layer Deposition (Al/Ni/Au) - 1:01

Equipment	*ID #*	*Procedure*	*P1*	*P2*	*P3*	*T1*	*T2*	*Notes*	*T0*
Pre-Clean - 0:09									
Develop Bench	1	Submount: 4 in. n-doped Si wafer						Fresh "prime" wafer (un-diced), with low resistivity	0:01:00
	2	Liquinox if neccesary; dump rinse 3x	Liquinox	DI	N_2			1 squirt, then fill beaker with water	0:01:00
PEII	3	Descum	300 mT	100 W		0:00:20			0:04:00
HF Bench	4	Native Oxide strip	BHF			0:01:00			0:02:00
Metal Deposition - 0:52									
Ebeam 3/4	5	Load Si wafer							0:01:00
	6	**50/50 nm Al/Ni**	500/500 Å	1,2 Å/sec		*0:08:00*	*0:08:00*	n-contact to Si	0:05:00
	7	**400 nm Au**	4 kÅ	1,3,5 Å/sec		*0:20:00*			0:05:00
µscope	8	Inspect deposition							0:05:00

[Si Sub-mount] Lithography (LOL1000/SPR220-7.0) - 3:42									
Equipment	***ID #***	***Procedure***	***P1***	***P2***	***P3***	***T1***	***T2***	***Notes***	***T0***
Pre-Clean - 0:10									
Solvent Bench	9	Clean Si submount wafer	Acetone	IPA		0:01:00	0:01:00		0:01:00
	10	Dump rinse 3x & dry	DI	N_2		0:01:00	0:01:00		0:01:00
PEII	11	Descum	300 mT	100 W		0:00:20			0:04:00
PR Spin - 0:27									
PR Bench	12	Setup hotplates	50 °C	200 °C					0:01:00
	13	Dehydration bake; let cool	200 °C			0:02:00	0:01:00		0:01:00
	14	**Spin underlayer, Recipe #5: ~80 nm**	LOL1000	3 krpm		0:00:30		Puddle in center, do not let liquid drip over wafer edge	0:01:00
	15	Use damp swab to remove edge bead	EBR100	3 krpm		0:00:30		hold against edge while spinning	0:01:00
	16	Soft Bake	200 °C			0:05:00		Set dissolution rate: ... slow	0:01:00
	17	Setup new wipes in spinner bowl						vapor will contaminate PR spin	0:01:00
	18	**Spin PR, Recipe #2: ~14.25 µm thick**	SPR220-7.0	1 krpm		0:00:45		Pour into center, do not let liquid drip over wafer edge	0:01:00
	19	Use damp swab to remove edge bead	EBR100	1 krpm		0:00:45			0:01:00
	20	Start soft bake	50 °C			0:00:30			0:01:00
	21	Increase temp and hold	115 °C			0:06:00		Ramp temp w/ wafer, hold after temp stable	0:01:00

Stepper Lithography - 2:46									
GCA AutoStep 200	22	Login						"L I [10,3]"	0:01:00
	23	Move robot to loading position						"RMSL"	0:01:00
	24	Load mask plate "NCONT"						Load chrome-side down and rotated 180°	0:05:00
	25	Take inventory						<CR> after "RMSL", or "INV"	0:01:00
	26	Prgm chuck size: "CHUCK -> C -> 100 -> Q"							0:02:00
	27	Edit prgm EGCLD: COL/ROW	3 rows	47 col					0:02:00
	28	Edit prgm EGCLD: Alignment Keys	standard						0:02:00
	29	Edit pass EGCLD\NPAD: pass shift	x = 0	y = -0.15 mm					0:02:00
	30	Edit pass EGCLD\NPAD: exposure, offset	3.2 sec	+0 offset					0:02:00
	31	Run "SETUP"							0:02:00
	32	Load Si wfr on chuck w/ shim	4" 500 µm	no shim				align wafer with flat at the top	0:03:00
	33	Change chuck size in software	100					"CHUCK" -> "C" -> "100" -> "Q"	0:01:00
	34	Load chuck on stepper stage						turn on stage vacuum	0:01:00
	35	Align and expose: "EXEC EGCLD\NPAD"	3.2 sec	+0 offset		0:00:03		no alignment	0:05:00
	36	Unload mask						"RMSR", "RMSL", remove mask, <CR>	0:01:00
	37	Unload chuck and wafer						"LOAD"; turn off stage & chuck vacuums	0:01:00
DUV Flood Expose	38	Cut square Al foil mask						100 mm x 100 mm to fit wafer	0:05:00
	39	Cut 4 square notches						10 mm x 10 mm notches, centered on each side	0:02:00
	40	Flood expose wafer				0:03:00		Use Al foil mask	0:02:00
	41	Let samples outgas				2:00:00		allows water vapor to absorb and complete reaction	0:01:00
	42	NO Post Expose Bake!						PR is too thick, will crack	0:01:00

PR Develop - 0:19									
Develop Bench	43	**Develop**, checking undercut often	AZ300MIF			0:05:00	0:00:15	develop 15 sec after PR done for minimal/no undercut!	0:01:00
	44	Dump rinse 3x & dry	DI	N_2		0:01:00	0:01:00		0:01:00
µscope	45	Inspect						Develop longer if necessary to clear pattern	0:05:00
Dektak	46	Dektak						Record step height.	0:05:00

[Si Sub-mount] Thick Plating (Au) - 6:23

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
PR Descum - 0:09									
PEII	47	Mount on blue tape						for backside protection; minimize air bubbles	0:04:00
	48	PR Descum: 60 nm	300 mT	100 W		0:01:00			0:04:00
Au Plating - 6:14									
Au Plating	49	Turn off pump							0:01:00
	50	Check water level; fill if necessary						< 1" from top; spray behind bath to avoid O_2 introduction	0:05:00
	51	Turn on pump and heater							0:01:00
	52	wait for temp. stabilization	55 °C						4:00:00
	53	calculate current	0.002 A/cm^2	~10.2 cm^2	~ 2.041 mA			surface area ~ 618.5 + Al foil-masked notches	0:02:00
	54	set time	6214 sec					rate: 1 µm / 478 sec; thickness: 13 µm	0:02:00
	55	load wafer on tray							0:02:00
	56	Check wafer-to-pin resistance	< 2 Ω					wiggle clip if necessary to get better contact	0:05:00
	57	lower wafer into bath, allow to etch				0:00:30			0:01:00
	58	**Start plating: 13 µm Au**				1:43:34			0:01:00
	59	Stop program and remove tray from bath						plating will continue if not stopped!	0:01:00
	60	rinse tray over bath	DI					minimize spread of etchant	0:02:00
	61	remove wafer, rinse thoroughly, dry	DI	N_2				remove blue tape	0:02:00
µscope	62	Inspect deposition							0:05:00

[Si Sub-mount] Seed Layer Wet Etch (Au) - 1:09									
Equipment	***ID #***	***Procedure***	***P1***	***P2***	***P3***	***T1***	***T2***	***Notes***	***T0***
PR Strip - 0:26									
Solvent Bench	63	**Strip photoresist**	1165			0:05:00		hold wafer over solvent drain and rinse with spray b	0:01:00
	64	**Strip**, sonicate on low	1165	80 °C		0:05:00		Use fresh beaker of stripper	0:01:00
	65	Dump rinse 3x & dry	DI	N_2		0:02:00	0:01:00		0:01:00
µscope	66	Inspect, repeat 1165 if necessary							0:05:00
Dektak	67	Measure height of Dektak mark						Record step height.	0:05:00
Metal Wet Etch - 0:43									
Acid Bench	68	**Strip 400 nm Au**	Etchant TFA			0:05:00		rate = 2.8 nm/sec @ 25 °C; http://transene.com/etchants/	0:05:00
	69	Dump rinse 3x & dry	DI	N_2		0:02:00	0:01:00		0:01:00
	70	**Strip 50 nm Ni**	Etchant TFB			0:00:30		rate = 3 nm/sec @ 25 °C; http://transene.com/etchants/	0:05:00
	71	Dump rinse 3x & dry	DI	N_2		0:02:00	0:01:00		0:01:00
	72	**Strip 50 nm Al**	Type A			0:00:30		rate = 3 nm/sec @ 25 °C; http://transene.com/etchants/	0:05:00
	73	Dump rinse 3x & dry	DI	N_2		0:02:00	0:01:00		0:01:00
µscope	74	Check pattern fidelity							0:05:00
Dektak	75	Measure height of Dektak mark						Record step height.	0:05:00

[Si Sub-mount] Carrier Wafer Dice - 0:54									
Equipment	***ID #***	***Procedure***	***P1***	***P2***	***P3***	***T1***	***T2***	***Notes***	***T0***
PR Spin - 0:09									
PR Bench	76	**Spin underlayer, Recipe #5: ~80 nm**	LOL1000	3 krpm		0:00:30		Puddle in center, do not let liquid drip over wafer edge	0:01:00
	77	Use damp swab to remove edge bead	EBR100	3 krpm		0:00:30		hold against edge while spinning	0:01:00
	78	Soft Bake	170 °C			0:05:00			0:01:00
Dice Wafer - 0:24									
Dicing Saw	79	Mount blade and flange	...-4C-30RU-3	53 mm					0:05:00
	80	Run "System Init"							0:03:00
	81	Mount wafer on tape						mount w/Si side on tape	0:01:00
	82	"Define Job": "speck\Nedy - carrier wafer"							0:01:00
	83	Load wafer							0:01:00
	84	Align sample using Au marks on Si							0:01:00
	85	Define 1st cut	+ 12.85 mm					top global alignment mark + 12.85 mm;	0:01:00
	86	Change alignment mode to 2nd angle							0:01:00
	87	Align sample using Au marks on Si							0:01:00
	88	Define 1st cut						align to edge of plated Au	0:01:00
	89	Inspect top and bottom cuts						scroll by die index	0:01:00
	90	Change alignment mode to 1st angle							0:01:00
	91	Run manual wafer y offset						align blade above wafer	0:01:00
	92	Run automated full wafer dicing prgm							0:01:00
	93	Clean wafer with water spray						Be sure to clean dicing gaps	0:01:00
	94	Unload wafer and blow dry	N_2						0:01:00
	95	UV expose tape/wafer				0:02:00			0:01:00
	96	Cut tape around wafer						easy storage in fluoroware	0:01:00
PR Strip - 0:21									
Solvent Bench	97	Remove a diced carrier from tape							0:01:00
	98	**Strip photoresist**	1165			0:05:00		hold wafer over solvent drain and rinse with spray b	0:01:00
	99	**Strip**, sonicate on low	1165	80 °C		0:05:00		Use fresh beaker of stripper	0:01:00
	100	Dump rinse 3x & dry	DI	N_2		0:02:00	0:01:00		0:01:00
µscope	101	Inspect, repeat 1165 if necessary							0:05:00

[Si] Clamping Wafer Dice - 1:06

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
Get wafers - 0:06									
Dicing Saw	102	Find wafer (pieces) of correct thickness	300-500 µm	500-800 µm	700-1100 µm			Correspond to the 3 LD-bar hieghts: 1/2 x to < 1 x	0:05:00
	103	Drop gauge thicknesses & record							0:01:00
Dice Wafer - 1:00									
Dicing Saw	104	Mount blade and flange	...-4C-30RU-3	53 mm					0:05:00
	105	Run "System Init"							0:03:00
	106	Mount one wafer on tape							0:01:00
	107	"Define Job": "speck\Nedy - carrier wafer"							0:01:00
	108	Load wafer							0:01:00
	109	Align sample along longest edge						Zero y to top of Si piece and x to the furtherst right edge	0:01:00
	110	Run manual wafer y offset 3 times	(0,1) mm	(0,6) mm	(0,11) mm				0:01:00
	111	Select the angle 90/2; align rotation						use default alignment	0:01:00
	112	Zero camera alignment						Zero y to top of previous cuts and x to the furthest right edge	0:01:00
	113	Run manual wafer y offset 3 times	(0,1) mm	(0,21) mm	(0,41) mm				0:01:00
	114	Clean wafer with water spray						Be sure to clean dicing gaps	0:01:00
	115	Unload wafer and blow dry	N_2						0:01:00
	116	UV expose tape/wafer				0:02:00			0:01:00
	116	Unload the six clamping pieces						Store for later use as workpiece clamps during polis	0:01:00
	117	Repeat for the remaining 2 wafers						Store for later use as workpiece clamps during polis	0:40:00

Quick Test - 2:02									
Equipment	***ID #***	***Procedure***	***P1***	***P2***	***P3***	***T1***	***T2***	***Notes***	***T0***
Defect Inspect - 0:15									
Florescence µscope	118	Record snapshots of defects	color uniformity	MFD's	DTD's			"misfit dislocations"; "dark triangles of death"	0:15:00
Photo-luminescence - 0:12									
GaN PL setup	119	Load reference	5 ms	B.C. = 5	avg = 5				0:01:00
	120	Remove dark spectrum							0:01:00
	121	Turn on laser, check alignment	40 mA						0:01:00
	122	Calib. to ref.; maximize intensity	~40 k					Record "correction factor" compared to P1	0:03:00
	123	Turn off, remove DS, turn on							0:01:00
	124	Load sample, maximize	10 ms	B.C. = 5	avg = 5			Should not require much adjustment	0:03:00
	125	set peak properties	width = 5					menu button on lower left	0:01:00
	126	record max and FWHM						multiply max by c.f.	0:01:00
Activate - 0:16									
Atmospheric Ovens	127	Timed Bake	600C			0:15:00			0:01:00
Electro-luminescence* - 0:49									
GaN EL setup	128	Screen **print Indium** on sample						Careful not to break sample; use one wipe	0:05:00
	129	Scrape excess In w/razor blade						Try not to smear In into holes w/o sample below	0:03:00
	130	**Solder Indium** on corner	bottom right			0:00:03		top&side of sample; hold for T1 to melt all In	0:05:00
	131	Load sample, position probes							0:03:00
	132	Turn on source, current limited	20 mA	20 V				No "burn-in"!	0:01:00
	133	Adjust fiber optic, max. intensity	10 ms	B.C. = 5	avg = 5			Record low power wavelength	0:05:00
	134	Turn on detector	450 nm					Low power wavelength from above	0:01:00
	135	Adjust detector, max. intensity						Record intensity and voltage	0:05:00
	136	Increase current source briefly	100 mA			0:05:00		Record high power wavelength quickly (heating)	0:01:00
	137	Adjust detector wavelength	450 nm					High power wavelength above	0:01:00
	138	Switch source to current limited	100 mA			0:00:05		Record intensity and voltage quickly (heating)	0:01:00
	139	Repeat above LIV measmts 4x						All four quadrants and center	0:13:00
Indium Removal* - 0:30									
Acid Bench	140	Prepare boiling HCl for Aqua-Regia	75 mL	> 80 °C				set hotplate to >180 °C; cover with watch glass	0:05:00
	141	Add HNO_3 to HCl	25 mL	> 80 °C					0:01:00
	142	**Indium Etch**: boiling Aqua-Regia	HCl:HNO_3 = 3:1	> 80 °C		0:05:00			0:05:00
	143	Repeat boiling A-R, 2x	3:1	> 80 °C		0:05:00	0:05:00	use fresh mix each time	0:01:00
	144	Dump rinse 3x & dry	DI	N_2		0:01:00	0:01:00		0:01:00

Dielectric Protection Deposition (SiO_2) - 2:50

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
Pre-Clean - 0:39									
Solvent Bench	145	Clean w/heated 1165, sonicate on high	1165	80 °C		0:02:00			0:01:00
	146	Dump rinse 3x	DI			0:01:00			0:01:00
	147	Add Liquinox; dump rinse 3x & dry	Liquinox	DI	N_2	0:01:00	0:01:00	1 squirt, then fill beaker with water	0:01:00
µscope	148	Inspect sample						Check for dirt or surface imperfections	0:05:00
UV Ozone	149	Oxygen clean after solvent/detergent				0:20:00		Important for adhesion	0:01:00
HF Bench	150	Strip native oxide of **Si Monitor #1** and **GaN Monitor #1**	BHF			0:02:00		Use the same plane as the sample for **GaN Monitor #1**	0:01:00
	151	Dump rinse 3x	DI			0:01:00			0:01:00
SiO_2 Deposition - 2:11									
Ebeam #2	152	Mount sample on kapton tape						Avoids clip mark on sample	0:05:00
	153	Load **Si Monitor #1**, **GaN Monitor #1** and sample						Use Kapton tape on **Si Monitor #1** - allows for dektak after	0:05:00
	154	Pump down; set tooling factor & thickness	*~130*	< 4E-6 mTorr				P1 calc., tf: new tf = old tf * measured / expected	1:00:00
	155	**400 nm SiO_2**	4 kÅ	2-3 Å/sec	t.f. = 128	*0:44:00*		Slow dep rate to improve adhesion	0:05:00
Ellipsometer (JAW)	156	Measure **Si Monitor #1**	"Cauchy on Si"						0:01:00
	157	Check fit in Analysis	$\lambda > 350$ nm	$\lambda < 1600$ nm				Record thickness and refractive index @ {450 nm, 632.8nm}	0:01:00
Dektak	158	Measure **Si Monitor #1**						Record height of Kapton tape lift-off	0:05:00
µscope	159	Inspect sample						Check for dirt or surface imperfections	0:05:00

GaN Backside Lithography (SF11/NR9-1000PY) - 1:43

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
Pre-Clean - 0:08									
Solvent Bench	160	Clean sample and submount	Acetone	IPA		0:01:00	0:01:00	Submount: 1 sq. inch Si diced; sonicate on low	0:01:00
	161	Dump rinse 3x	DI			0:01:00			0:01:00
	162	Add Liquinox; dump rinse 3x & dry	Liquinox	DI	N_2	0:01:00	0:01:00	1 squirt, then fill beaker with water	0:01:00
PR Spin - 0:48									
PR Bench	163	Dehydration bake	180 °C			0:02:00		sample is still upside down	0:02:00
	164	Mount GaN on blue tape, upside down						corral with DSP sapphire in spiral pattern	0:05:00
	165	**Spin underlayer: ~0.9 µm thick**	SF11	5 krpm	10 krpm/s	0:00:30			0:01:00
	166	Unmount; clean topside	EBR100						0:10:00
	167	Soft bake	180 °C			0:02:00		sample is still upside down	0:01:00
	168	Setup new wipes in spinner bowl						vapor will contaminate PR spin	0:01:00
	169	Mount GaN on blue tape, upside down						corral with DSP sapphire in spiral pattern	0:05:00
	170	**Spin PR 778 nm thick**	NR9-1000PY	5 krpm	10 krpm/s	0:00:30			0:02:00
	171	Unmount; clean topside	EBR100						0:10:00
	172	Soft bake	115 °C			0:05:00		sample is still upside down; use lid (very sensitive to	0:01:00

Stepper Lithography - 0:33									
GCA AutoStep 200	173	Login						"L I [10,3]"	0:01:00
	174	Move robot to loading position						"RMSL"	0:01:00
	175	Load mask: "EGC_LD_v4_RIDGE{x}UM"						Load chrome-side down w/barcode in lower right corner	0:01:00
	176	Take inventory						<CR> after "RMSL", or "INV"	0:01:00
	177	Edit prgm EGCLD: COL/ROW	1 row	*7 col.*				# col. Based on width of sample ÷ 1.63 mm	0:02:00
	178	Edit prgm EGCLD: Alignment Keys	Right: R1C7	Left: R1C2					0:02:00
	179	Edit pass EGCLD\NCONT: pass shift	x = -1.065 mm	y = -0.15 mm					0:02:00
	180	Edit pass EGCLD\NCONT: exposure, offset	0.79	-3 offset					0:02:00
	181	Run "SETUP"							0:02:00
	182	Load sample on chuck w/ shim	2" 500 µm	180 µm				with C- pointing up; turn on chuck vacuum	0:03:00
	183	Change chuck size in software	7100					"CHUCK" -> "C" -> "7100" -> "Q"	0:01:00
	184	Load chuck on stepper stage						turn on stage vacuum	0:01:00
	185	Align and expose: "EXEC EGCLD\NCONT"	0.79	-3 offset				Align right screen to right edge, center of y	0:05:00
	186	Unload masks						"RMSR", "RMSL", remove masks, <CR>	0:01:00
	187	Unload chuck and wafer						"LOAD"; turn off stage & chuck vacuums	0:01:00
PR Bench	188	Let sample outgas				0:05:00			0:01:00
	189	Soft bake	115 °C			0:02:00			0:01:00

PR Develop - 0:14									
Develop Bench	190	**Develop** with 0.5 µm undercut	AZ300MIF			0:00:05	0:00:15	develop ~15 sec past where PR stops dissolving; undercut rate ~ 0.5 µm per 15 sec	0:01:00
	191	Dump rinse 3x & dry	DI	N_2		0:01:00	0:01:00		0:01:00
µscope	191	Inspect						Check undercut, develop longer if necessary	0:05:00
Dektak	192	Dektak						Record step height.	0:05:00

n-Contact Deposition (Ti/Al/Ni/Au) & Lift-Off - 1:26									
Equipment	***ID #***	***Procedure***	***P1***	***P2***	***P3***	***T1***	***T2***	***Notes***	***T0***
PR Descum - 0:10									
PEII	193	PR Descum: 60 nm	300 mT	100 W		0:01:00			0:04:00
Acid Bench	194	Native oxide strip of sample	HCl:DI = 1:3			0:00:30			0:01:00
	195	Dump rinse 3x & dry	DI	N_2		0:01:30	0:01:00		0:01:00
Metal Deposition - 0:56									
Ebeam 3/4	196	Tape sample and **Si Monitor #2** to flat stage						Use Kapton tape on GaN edges to assist with lift-off; Ebeam 3: align c-direction left-to-right on stage	0:01:00
	197	**35/115/150 nm Ti/Al/Ni**	350/1150/1500 Å	1,2 Å/sec		0:20:00			0:05:00
	198	**300 nm Au**	3 kÅ	1,3,5 Å/sec		0:15:00			0:05:00
µscope	199	Inspect deposition							0:05:00
Dektak	200	Dektak **Si Monitor #2**						Record step heights. ***Si Monitor #2 COMPLETE***	0:05:00
Lift-Off - 0:20									
Solvent Bench	201	**Strip photoresist,** sonicate on low	1165	80 °C		0:05:00		Drop into heated beaker & sonicating beaker; Be sure that sample is epi-side up to prevent re-deposition	0:01:00
	202	**Strip**, sonicate on low	1165	80 °C		0:05:00		Use fresh stripper; drop into heated sonicating beak	0:01:00
	203	Dump rinse 3x & dry	DI	N_2		0:01:30	0:01:00		0:01:00
µscope	204	Inspect: complete LO						Repeate LO if necessary	0:05:00

Substrate:Sub-mount Bond (Au-Au) - 1:53									
Equipment	***ID #***	***Procedure***	***P1***	***P2***	***P3***	***T1***	***T2***	***Notes***	***T0***
Sample Prep - 0:28									
Drop Gauge	205	Measure & record thicknesses						sample, carrier, DSP sapphire *m* -plane ~ 330 µm, 20-2-1 ~ 350 µm, DSP sapp. ~ 430 µm	0:04:00
Develop Bench	206	Swab with detergent	Liquinox	DI				Both sample and carrier	0:04:00
	207	Scrape surface with razor blade						Both sample and carrier; keep sample wet	0:04:00
	208	Swab	Liquinox	DI				Both sample and carrier	0:04:00
	209	Dump rinse 3x	DI			0:01:00			0:01:00
	210	Add Liquinox; dump rinse 3x & dry	Liquinox	DI	N_2	0:01:00	0:01:00	1 squirt, then fill beaker with water	0:01:00
PEII	211	Descum after detergent	300 mT	100 W		0:03:00		Both sample and carrier	0:04:00
Au-Au Bond - 0:56									
FineTech Flip-Chip Bonder	212	Switch out arm w/ High Force Arm						arm and festo	0:15:00
	213	Install 0x0 backing plate						zero out rotation	0:05:00
	214	Install 15x15 tooling, with shims	*.67 mm*					Only tooling with a gimbal; shims + sample = 1 mm	0:02:00
	215	Focus camera using stage height							0:02:00
	216	Place DSP sapphire on stage, rough align							0:01:00
	217	De-focus stage by height difference						move stage down by DSP sapp. height - sample height	0:01:00
	218	Calibrate vacuum with out sample						Be sure to update ALL profiles	0:01:00
	219	Run "HFA Pick n Place"							0:02:00
	220	Calibrate vacuum with sample on tooling						Be sure to update ALL profiles	0:01:00
	221	Run "HFA Pick n Place"							0:02:00
	222	Run "Gimbal Align"	400 N			0:00:30		press tooling into sample to level gimbal	0:02:00
	223	Place Si on stage & rough align						Focus camera on Si using stage height	0:05:00
	224	Run "HFA Pick n Place"						pick up the GaN piece with the tooling	0:01:00
	225	Rough align sample to Si submount							0:05:00
	226	Run "HFA Pick n Place" to pick up sample							0:01:00
	227	Align sample and submount						sample focus is adjustable	0:05:00
	228	Run "HFA Pick n Place" to place sample						monitor placement and vacuum control	0:01:00
	229	Run "HFA Pick n Place" to pick up sample							
	230	Check alignment							0:01:00
	231	Run "HFA Au-Au Bond"	400 N	330 °C		0:00:20	0:00:40	Ramp temp. before placement Check alignment during temp stabilize arm down (T1), ramp temp. down with pressure (T2)	0:01:00
	232	Switch out arm w/ Low Force Arm						arm and festo	0:01:00

n-Contact Anneal - 0:29									
RTA	233	Place sample on RTA carrier						GaN-side up	0:05:00
	234	Place thermocouple on Si sub-mount							0:01:00
	235	Anneal	450 °C	0.5 mTorr		0:03:00			0:15:00
	236	Unload after cooling	< 100 °C						0:05:00

Dielectric Hard Mask Deposition (SiO_2) - 3:00

Equipment	*ID #*	*Procedure*	*P1*	*P2*	*P3*	*T1*	*T2*	*Notes*	*T0*
Pre-Clean - 0:49									
Solvent Bench	237	Clean with heated 1165	1165			0:05:00	0:05:00	Repeat 2x; no sonication	0:01:00
	238	Dump rinse 3x & dry	DI	N_2		0:01:00	0:01:00		0:01:00
µscope	239	Inspect sample for SiO_2 imperfections						CONTINUE/SKIP REWORK BASED ON INSPECTION	0:05:00
HF Bench	240	Time oxide etch of **Si Monitor #1**	BHF			*0:01:30*	0:00:10	Etch rate ~300 nm/min; after T1, check water beading of Si Monitor #1 every T2 and record total etch time. ***Si Monitor #1 COMPLETE***	0:01:00
	241	Dump rinse 3x	DI			0:01:00			0:01:00
	242	Timed oxide etch of sample and **Si Monitor #3**	BHF			*0:02:15*		Etch for 1.5x the recorded time for **Si Monitor #1**	0:01:00
	243	Dump rinse 3x	DI			0:01:00			0:01:00
UV Ozone	244	Oxygen clean sample				0:20:00		Important for adhesion	0:01:00
SiO2 Deposition - 2:11									
Ebeam #2	245	Mount sample on kapton tape						Avoids clip mark on sample	0:05:00
	246	Load **Si Monitor #3** and sample						Use Kapton tape on **Si Monitor #3** - allows for dektak after	0:05:00
	247	Pump down; set tooling factor & thickness	*~130*	< 4E-6 mTorr				P1 calc., tf: new tf = old tf * measured / expected	1:00:00
	248	**400 nm SiO_2**	4 kÅ	2-3 Å/sec	t.f. = 128	*0:44:00*		Slow dep rate to improve adhesion; calibrate tooling factor from SiO_2 thickness of **Si Monitor #1**	0:05:00
Ellipsometer (JAW)	249	Measure **Si Monitor #3**	"Cauchy on Si"						0:01:00
	250	Check fit in Analysis	$\lambda >$ 350 nm	$\lambda <$ 1600 nm				Record thickness and refractive index @ {450 nm, 632.8nm}	0:01:00
Dektak	251	Measure **Si Monitor #3**						Record height of Kapton tape lift-off	0:05:00
µscope	252	Inspect sample						Check for dirt or surface imperfections	0:05:00

Air Gap Electron Beam Lithography (A4 PMMA/HSQ) - 18:01

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
Pre-Clean - 0:18									
Solvent Bench	253	Clean with heated 1165	1165			0:05:00	0:05:00	Repeat 2x; no sonication	0:01:00
	254	Dump rinse 3x & dry	DI	N_2		0:01:00	0:01:00		0:01:00
PEII	255	Descum	300 mT	100 W		0:00:20			0:04:00
PR Spin - 0:18									
PR Bench	256	Get HSQ, 2% from fridge	HSQ, 2%					Let warm up for 10 min.	0:01:00
	257	Dehydration bake; let cool	180 °C			0:02:00	0:01:00	Use hot plate in Bay 7, next to 100 °C hot plate	0:01:00
	258	**Spin PMMA: ~ 190 nm thick** on sample and **GaN Monitor #1**	950k, A4	5 krpm	10krpm/s	0:00:40		thick PMMA - will shrink with exposure	0:01:00
	259	Bake sample and monitor	180 °C			0:05:00			0:01:00
	260	Use a syringe to get ~2.5 mL of HSQ	HSQ, 2%	2.5 mL				Flow constant light N_2 into bottle and cap	0:02:00
	261	**Spin HSQ: ~ 30 nm thick** on sample and **GaN Monitor #1**	HSQ, 2%	5 krpm	10krpm/s	0:00:30		use syringe and filter; 2.5 mL is enough	0:01:00
	262	Bake sample and monitor	100 °C			0:01:00			0:01:00
Metal Deposition - 0:15									
Thermal Evaporator #1	263	Load sample						Use kapton tape	0:01:00
	264	Load new tunsten boat	Al wire	slot #2				~ 20 winds around tweezer	0:01:00
	265	**10 nm Al** on sample and **GaN Monitor #1**	100 Å	0.5 Å/sec		0:03:20			0:05:00
	266	Unload and get to EB Litho						Al oxidizes quickly. Start EBL load lock venting befor	0:05:00

Load Sample & Calibrate Ebeam - 1:48									
JEOL 6300	267	Check lens, beam current, aperature	4th Lens	2 nA	60 µm			Mode 3: 100 keV...	0:01:00
	268	Start recharge timer						To record beam time	0:01:00
	269	Vent L/L, unload cassettes 2,4 & pump	cassette 2	cassette 4				vent w/handle up; pump w/handle down	0:05:00
	270	Load sample on stage	stage 2E					22 mm wide stage on cassette 2	0:05:00
	271	Load **GaN Monitor #1** on stage	stage 2G					3 mm wide stage on cassette 4	0:05:00
	272	Align sample using alignment station						Align using the EB alignment marks	0:05:00
	273	Record sample position						Holder to left/right edge of sample; sample width	0:05:00
	274	Vent L/L; load cassettes; pump L/L						vent w/handle up; pump w/handle down	0:30:00
	275	Check JDF file: Array statements						x = (2*N-1) * 815; y = 0;	0:05:00
	276	Compile magazine file in terminal						"sched *.sdf". Use "dos2unix" first if necessary	0:02:00
	277	Check pattern						Analysis screen -> "ACHK"	0:10:00
	278	Check beam current, adjust w/ LENS 2/3						@ Faraday Cup	0:02:00
	279	Check stigmation						@ BE (Bottom Plane) mark	0:05:00
	280	Check beam current if stig changed						@ Faraday Cup; see manual: Section 6 for more detail	0:02:00
	281	Move to AE (Bottom Plane) mark							0:01:00
	282	Run "INITAE", then "SFOCUS"							0:05:00
	283	If |STIG| > 10, rerun						Run --/SXX/SYY if needed. See manual for more detail	0:03:00
	284	Move to BE (Bottom Plane) mark							0:02:00
	285	Run automated batch calibration						"Commands -> Batch -> Input File... -> 4th_DEFLECTOR"	0:06:00
	286	Save condition						"SAVE - > Edit Parameter -> Acquisition of ... -> Apply"	0:02:00
	287	Record LENS values	LENS2	LENS4					0:01:00
	288	Record values for height offset	PDEF	SUBDEF				"INIEBX -> Acquisition of... -> {HCOEFFI} Setting" See instruction manual: Section 6.8 (addendum)	0:05:00

Ebeam Lithography - 15:12									
JEOL 6300	289	Change stage settings						"Mutliwafer: 2E" and "Substrate"	0:01:00
	290	Find 1.2 mm Au pad @ holder edge						~ ((+/-) 11000, 0) µm	0:05:00
	291	Move to GaN edge						Use recorded offset to move	0:02:00
	292	Focus on nearest defect on sample	R1C1	LENS4'				Avoid exposing first die; record new LENS4	0:10:00
	293	Reset LENS4 and turn off SEM	LENS4						0:01:00
	294	Modify SDF file with xy & height offset						Use "EBL Offset Calculator.xlsx"	0:05:00
	295	Check JDF file: Array statements						x = (2*N-1) * 815; y = 0;	0:05:00
	296	Compile magazine file in terminal	sched *.sdf					Use "dos2unix" program first if necessary	0:02:00
	297	Stop SEM and recharge timer						Record time in log book	0:01:00
	298	Expose pattern	25k & 1k µC/cm^2	A2 & A4		*5:15:00*		Write gratings & align marks in separate layers; 45 min/die	0:01:00
	299	Load cassette 4 and repeat alignment							0:15:00
	299	Modify JDF with sparse die						Use a modified pattern with groups of 2 mm long gratings	3:00:00
	300	Modify SDF file with xy offset						No height offset	3:00:00
	300	Run litho on **GaN monitor #1**						A few die with space to cleave for dry etch calibrations	3:00:00
	301	Check exp. time when finished						Record time in log book	0:01:00
	302	Vent L/L; unload cassettes & samples						vent w/handle up	0:03:00
	303	Load cassettes and pump L/L						pump w/handle down	0:05:00

PR Develop - 0:10									
HF Bench	304	Develop	TMAH, 25%			0:01:00		Al removed in 30 sec.; develop HSQ in 30 sec	0:01:00
	305	Dump rinse 3x & dry	DI	N_2		0:01:00	0:01:00	Carefully, pattern is fragile	0:01:00
µscope	306	Inspect lithography						Look for 20 µm rectangles, spaced horizontally by 180 µm	0:05:00

Air Gap Hard Mask Deposition (Ti/Ni) & Lift-Off - 3:43

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
PMMA Etch - 0:47									
RIE 5	307	load cleaning wafer							0:05:00
	308	O2 clean - "NEDY_01"	100 W	50 mTorr	30 sccm	0:20:00			0:05:00
	309	load sample on wafer							0:05:00
	310	"NEDY_01: O2 PMMA etch"	100 W	50 mTorr	30 sccm	0:02:00		60 sec undercut, ~50 nm on each side	0:05:00
µscope	311	Inspect lithography							0:05:00
Ni Dep - 0:34									
Ebeam #3	312	Load sample, **GaN Monitor #1** & **Si Monitor #4**						Use angled stage to gun 1; mount **Si Monitor #4** w/Kapton tape	0:10:00
	313	**1 nm Ti**	10 Å	1 Å/sec		0:00:30		Make sure pressure is < 4e-7 before dep.	0:04:00
	314	**30 nm Ni**	300 Å	1-3-5 Å/sec		0:01:15		5 sec ramp after 5 Å, 5 sec ramp after 15 Å	0:04:00
µscope	315	Inspect Dep							0:05:00
Dektak	316	Dektak **Si Monitor #4**						Record step height.	0:05:00
	317	Dektak RIDGES pad						Record step height.	0:05:00
Lift-Off - 2:21									
Solvent Bench	318	**Strip resist** off sample and **GaN Monitor #1**	1165	80 °C		2:00:00		Dip into heated beaker and soak in heated bath; Make sure sample is epi-side down to prevent re-deposition	0:01:00
	319	**Strip resist**	1165	80 °C		0:01:00		Use fresh stripper; agitate with pipette	0:01:00
	320	Dump rinse 3x & dry	DI	N_2		0:01:30	0:01:00		0:01:00
SEM	321	Inspect: complete LO						Repeate LO if necessary	0:15:00

Air Gaps Dry Etch (SiO2 & GaN) - 10:45

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
PR Descum - 0:04									
PEII	322	PR Descum: 20 nm	300mT	100W		0:00:20			0:04:00
SiO2 Dry Etch - 1:00									
ICP #2	323	*Gas line vacuum & gas change: SF_6 -> CF_4*				*0:03:00*		*if necessary*	*0:03:00*
	324	*Etch test recipes: 109*				*0:03:00*		*if necessary*	*0:03:00*
	325	Clean & load O_2 cleaning wafer	Acetone	IPA	DI/N2			Clean & check backside	0:05:00
	326	O_2 clean, Recipe: 103	40 sccm	900/100 W	5.0 Pa	0:05:00			0:02:00
	327	Clean & load seasoning wafer	Acetone	IPA	DI/N2			Clean & check backside	0:05:00
	328	Season with #126: "DielectricNano"	CF_4 = 40 sccm	900/50 W	0.5 Pa	0:03:40		Check recipe, it's changed often	0:02:00
	329	Clean & load etch carrier wafer w/sample	Acetone	IPA	DI/N2			Do not use Santovac oil to mount	0:05:00
	330	400 nm SiO_2 Etch, #126: "DielNano" on sample and **GaN Monitor #1**	CF_4 = 40 sccm	900/50 W	0.5 Pa	0:03:40		SiO2 etch rate = 120 nm/min GaN etch rate = 14 nm/min; d ~ 5 nm	0:02:00
	331	Load O_2 cleaning wafer							0:01:00
	332	O_2 clean, Recipe: 103	40 sccm	900/100 W	5.0 Pa	0:07:00			0:02:00
	333	Unload carrier, unmount sample	Acetone	IPA	DI				0:05:00
Hard Mask Strip - 0:07									
Acid Bench	334	Nickel etch of **Si Monitor #4**	Etchant TFB			0:00:10	0:05:00	Etch rate: 3 nm/sec; visually inspect, etch more if necessary; ***Si Monitor #4 COMPLETE***	0:04:00
	335	30 nm nickel etch of sample & **GaN Monitor #1**	Etchant TFB			*0:00:25*		Etch rate: 3 nm/sec; overetch by 100% of **Si Monitor #4**	0:04:00
	336	Dump rinse 3x & dry	DI	N_2		0:01:00	0:01:00		0:01:00

GaN Dry Etch - 5:19									
Unaxis Etch	337	Clean & load wfrs: Sapp., Si, Ni	Acetone	IPA	DI/N2				0:05:00
	338	Cl_2 clean: "Nedy Fast Etch-200C"				0:05:00		On sapp. wafer	0:15:00
	339	"O2-clean 60min-200C"	50 sccm	800/200 W	10 mTorr	1:00:00		On Si wafer	0:15:00
	340	Load Ni carrier w/ GaN dummies							0:05:00
	341	BCl_3 & Cl_2/Ar Season: "Nedy PhC GaN Season-200C"	50 sccm 10/10 sccm	500/50 W 200/5 W	10 mTorr 2 mTorr	0:01:40	0:15:00		0:15:00
	341	Mount cleave of **GaN Monitor #1** on **Si Monitor #5** w/grease	Corning High Vacuum Grease					Cleave small (~ 1 mm) pieces along c-direction	0:05:00
	342	Load Ni carrier wafer monitors						Use same 2" GaN dummy from season to cover exposed Si	0:05:00
	343	**25 nm + *650 nm*** BCl_3 & Cl_2/Ar **etch** : "Nedy PhC GaN Etch-200C"	50 sccm 10/10 sccm	500/50 W 200/5 W	10 mTorr 2 mTorr	0:01:40	*0:14:37*	SiNx etch rate: 6nm/min, 352.8nm/min Al2O3 etch rate: 28.2nm/min, ~0 50/50 PhC GaN etch rate: 15nm/min, 46.8nm/min Planar GaN etch rate: 45nm/min, 44.4nm/min	0:15:00
	344	Un-mount cleave of **GaN Monitor #1**	Acetone	IPA	DI/N2			**Si Monitor #5 COMPLETE**	0:05:00
SEM	345	SEM cleave of **GaN Monitor #1**	SEI	15 kV				Cleave etched piece in half to view cross-section	0:10:00
	346	Record grating profile and depth						Modify etch time/parameters & repeat etch test if necessary; **GaN Monitor #1 COMPLETE**	1:30:00
Unaxis Etch	347	Load Ni carrier wafer w/dummy and mount sample w/grease	Corning High Vacuum Grease					Use same GaN dummies from season to cover exposed Si	0:05:00
	348	**25 nm + *650 nm*** BCl_3 & Cl_2/Ar **etch** : "Nedy PhC GaN Etch-200C"	50 sccm 10/10 sccm	500/50 W 200/5 W	10 mTorr 2 mTorr	0:01:40	*0:14:37*	SiNx etch rate: 6nm/min, 352.8nm/min Al2O3 etch rate: 28.2nm/min, ~0 50/50 PhC GaN etch rate: 15nm/min, 46.8nm/min Planar GaN etch rate: 45nm/min, 44.4nm/min	0:15:00

ALTERNATE GaN Dry Etch - 0:30									
ICP #2	349	*Gas line vacuum & gas change: CHF_3 -> Ar*				*0:03:00*		*if necessary*	*0:03:00*
	350	*Etch test recipes: 102*				*0:03:00*		*if necessary*	*0:03:00*
	351	O_2 clean on cleaning wafer, Recipe: 103	40 sccm	900/100 W	5.0 Pa	0:05:00			0:02:00
	352	Change recipe 186 to "LP GaN"	22.5/22.5 sccm	250/30 W	0.2 Pa	0:15:00		Extra ignition step (#3): ICP/forward = 250/30 W, 0 sec	0:05:00
	351	Clean & load Ni carrier wafer w/dummies							0:05:00
	353	Cl_2/Ar Season, 186: "LP GaN"	22.5/22.5 sccm	250/30 W	0.2 Pa	0:15:00			0:15:00
	353	Mount cleave of **GaN Monitor #1** on **Si Monitor #5** w/grease	Corning High Vacuum Grease					Cleave small (~ 1 mm) pieces along c-direction	0:05:00
	354	Load Ni carrier wafer monitors						Use same 2" GaN dummy from season to cover exposed Si	0:05:00
	355	**675 nm** Cl2/Ar **etch**, 186 : "LP GaN" on **GaN Monitor #1**	22.5/22.5 sccm	250/30 W	0.2 Pa	*0:10:41*		SiNx etch rate: 6nm/min, 352.8nm/min Al2O3 etch rate: 28.2nm/min, ~0 50/50 PhC GaN etch rate: 15nm/min, 46.8nm/min Planar GaN etch rate: 45nm/min, 44.4nm/min	0:15:00
	356	Un-mount cleave of **GaN Monitor #1**	Acetone	IPA	DI/N2			**Si Monitor #5 COMPLETE**	0:05:00
SEM	357	SEM cleave of **GaN Monitor #1**	SEI	15 kV				Cleave etched piece in half to view cross-section	0:10:00
	358	Record grating profile and depth						Modify etch time/parameters & repeat etch test if necessary; **GaN Monitor #1 COMPLETE**	1:30:00
ICP #2	359	Load Ni carrier wafer w/dummies and mount sample with oil	Santovac Oil					Use same GaN dummies from season to cover exposed Si	0:05:00
	360	***675 nm*** Cl_2/Ar **etch**, 186 : "LP GaN" of sample	22.5/22.5 sccm	250/30 W	0.2 Pa	*0:10:40*		SiO_2 etch rate: 12 nm/min 50/50 PhC *m* -plane GaN etch rate: 63 nm/min	0:15:00

Ridges Lithography (HMDS/SPR220-7.0) - 2:03

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
Pre-Clean & Corral - 0:11									
Solvent Bench	361	Clean	Acetone	IPA		0:01:00	0:01:00	No sonication	0:01:00
	362	Dump rinse 3x	DI			0:01:00			0:01:00
Develop Bench	363	Add Liquinox; dump rinse 3x & dry	Liquinox	DI	N_2	0:01:00	0:01:00	1 squirt, then fill beaker with water	0:01:00
Solvent Bench	364	Spread crystal bond on carrier	Crystal Bond	Acetone				Use wood handle of swab to dab crystal bond/acetone mix in thin square around sample	0:01:00
	365	Corral w/DSP sapphire rectangles						Corral substrate tightly using a swastika pattern	0:01:00
PR Bench	366	Ramped bake	95 °C	105 °C	115 °C	0:00:30		Keep corral tight while heating	0:01:00
PR Spin - 0:30									
PR Bench	367	Prepare hotplates	50 °C					Use Al cups as lid	0:01:00
	368	Dehydration bake, let cool	115 °C			0:02:00	0:01:00		0:02:00
	369	Mount carrier w/GaN on blue tape							0:05:00
	370	**Adsorb & spin adhesion promoter**	HMDS	5 krpm	10 krpm/s	0:00:40	0:00:30		0:01:00
	371	**Spin PR ~5.5 µm thick**	SPR220-7.0	5 krpm	10 krpm/s	0:00:30			0:02:00
	372	Unmount; clean topside	EBR100					If necessary	0:10:00
	373	Start soft bake	50 °C			0:01:00			0:01:00
	374	Increase temp and remove corral	95 °C					carefully pull corral off carrier after crystal bond is melted	0:01:00
	375	Increase temp and hold	115 °C			0:02:00		Ramp temp w/ wafer, cover w/ lid & hold after temp	0:01:00

Stepper Lithography - 1:02									
GCA AutoStep 200	376	Login						"L I [10,3]"	0:01:00
	377	Move robot to loading position						"RMSL"	0:01:00
	378	Load mask: "EGC_LD_v4_RIDGE{x}UM"						load w/barcode in lower right corner	0:01:00
	379	Take inventory						<CR> after "RMSL", or "INV"	0:01:00
	380	Edit prgm EGCLD: COL/ROW	1 row	*7 col.*				# col. Based on width of sample ÷ 1.63 mm, plus 2	0:02:00
	381	Edit prgm EGCLD: Alignment Keys	*Right: R1C7*	*Left: R1C3*				Be sure that die R1C1 and R1C2 are off the wafer	0:02:00
	382	Edit pass EGCLD\RIDGE: barcode	*RDG-P 6UM*					barcode corresponds to mask	0:01:00
	382	Edit pass EGCLD\RIDGE: pass shift	x = 0	y = 0					0:02:00
	383	Edit pass EGCLD\RIDGE: exp., offset	1.05 sec	0				Slight over-exposure to compensate for edge bead	0:01:00
	384	Run "SETUP"							0:02:00
	385	Load sample on chuck, no shim	Black Multi					with C- pointing up; turn on chuck vacuum	0:03:00
	386	Change chuck size in software	7100					"CHUCK" -> "C" -> "7100" -> "Q"	0:01:00
	387	Load chuck on stepper stage						turn on stage vacuum	0:01:00
	388	Run focus & expose passes						"EXEC EGCLD" -> "FOCUS, RIDGE"	0:01:00
	389	Align and expose						align right key first, left key for theta	0:05:00
	390	Record voltages for manual focus						during "FOCUS" pass	0:05:00
	391	Turn to manual column height control						between "FOCUS" and "P-CONT" passes	0:01:00
	392	Set manual focus and expose each die						First die should fail; set focus before each die is exposed; For edge die, average the recorded value and its neighbor	0:05:00
	393	Abort and unload masks						"Ctrl + c -> a","RMSR", "RMSL", remove masks, <CR>	0:01:00
	394	Unload sample						"LOAD"; turn off stage & chuck vacuums	0:01:00
PR Bench	395	Hold before PEB				0:20:00		Important to let water diffuse back in to complete e	0:01:00
	396	Start soft bake	50 °C			0:01:00			0:01:00
	397	Increase temp and hold	115 °C			0:02:00		Ramp temp w/ wafer, cover w/ lid & hold after temp	0:01:00

PR Develop - 0:16									
Develop Bench	398	**Develop**	AZ300MIF			0:02:00		Very light agitation	0:01:00
	399	Dump rinse 3x & dry	DI	N_2		0:01:00	0:01:00	Careful, thick PR is very fragile	0:01:00
µscope	400	Inspect							0:05:00
Dektak	401	Dektak						Do not dektak ridges! Record step height of dektak	0:05:00

Ridges Dry Etch (SiO2 & GaN) - 4:03

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
PR Descum - 0:04									
PEII	402	**PR Descum: 20 nm**	300 mT	100 W		0:00:20		~1 nm/sec	0:04:00
SiO2 & GaN Dry Etch - 2:16									
ICP #2	403	Gas change & gas line vacuum: *SF_6 -> CF_4*				0:03:00		if necessary	0:03:00
	404	Etch test recipes: *109*				0:03:00		if necessary	0:03:00
	405	Gas change & gas line vacuum: *CHF_3 -> Ar*				0:03:00		if necessary	0:03:00
	406	Etch test recipes: *102*				0:03:00		if necessary	0:03:00
	407	Clean & load O_2 cleaning wafer	Acetone	IPA	DI/N_2			Clean & check backside	0:05:00
	408	O_2 clean, Recipe: 103	40 sccm	900/100 W	5.0 Pa	0:05:00			0:02:00
	409	Clean & load carrier wafer	Acetone	IPA	DI/N_2			Clean & check backside	0:05:00
	410	Season with #126	CF_4 = 40 sccm	900/50 W	0.5 Pa	0:03:40		Check recipe, it's changed often	0:02:00
	411	Load carrier wafer w/sample						Mount w/a drop of Santovac diffusion pump oil	0:05:00
	412	400 nm SiO_2 Etch, #126: "DielectricNano"	CF_4 = 40 sccm	900/50 W	0.5 Pa	0:03:40		SiO2 etch rate = 120 nm/min GaN etch rate = 14 nm/min SPR220-7.0 ~ 140 nm/min NR9-1000PY etch rate = 80 nm/min AZNLOF2020 etch rate = 242.4 nm/min	0:02:00
	413	Unload carrier, but do not unmount							0:05:00
	414	Clean & load seasoning wafer	Acetone	IPA	DI/N_2			Clean & check backside	0:05:00
	415	Change recipe 186 to "HP GaN"	60/60 sccm	175/600 W	1 Pa			With an extra bias ramp step (#3) of ICP/forward = 300/600 W	0:05:00
	416	Cl_2/Ar Season, 186: "HP GaN"	60/60 sccm	175/600 W	1 Pa	0:05:00			0:15:00
	417	Load carrier wafer w/sample							0:05:00
	418	***1.5 µm*** Cl_2/Ar **etch**, 186 : "HP GaN"	60/60 sccm	175/600 W	1 Pa	0:05:00		*m* -plane GaN etch rate: 473 nm/min SiO_2 etch rate: ~1.5 µm/min (?) SPR220-7.0 etch rate: 418 nm/min; corners etch ~2x faster!	0:15:00
	419	Load CF_4 cleaning wafer							0:01:00
	420	CF_4/O_2 clean, Recipe: 106	40/40 sccm	700/100 W	5.0 Pa	0:06:00			0:02:00
	421	Unmount sample						Slide horizontally to detach oil	0:05:00
	422	Clean oil off carrier wafer	Acetone	IPA	DI/N_2			Use a swab and limit excess solvent	0:05:00

PR Strip - 0:38									
Solvent Bench	423	**Strip photoresist** in heated bath	AZ300-T	80 °C		0:20:00		lay sample upside down in beaker/container	0:01:00
	424	**Strip**, agitate w/pipette	AZ300-T	80 °C		0:02:00		Use fresh beaker of stripper	0:01:00
	425	Cascade Dump rinse 3x & dry	DI	N_2		0:02:00	0:01:00		0:01:00
µscope	426	Inspect, repeat strip if necessary							0:05:00
Dektak	427	Dektak RIDGE pad						Record step height.	0:05:00

Inspect - 1:05									
µscope	428	Inspect ridges across wafer						Record width of ridges @ the four corners of each die	1:00:00
Dektak	429	Dektak RIDGE pad						Record step height.	0:05:00

Dielectric Passivation (BCB) - 10:06

Equipment	*ID #*	*Procedure*	*P1*	*P2*	*P3*	*T1*	*T2*	*Notes*	*T0*
Oven Prep - 0:05									
Blue M Oven	430	Check that oven is at 25°C	25 °C						0:01:00
	431	Confirm sequence for Program #5						See "Final Cure" steps	0:01:00
	432	Place Al baking table inside							0:01:00
	433	Purge: run N2 through chamber	N2	100%	0:30:00				0:01:00
	434	Set alarm	275 °C						0:01:00
Pre-Clean - 0:09									
UV Ozone	435	Oxygen clean				0:20:00			0:01:00
Acid Bench	436	Native Oxide strip of sample	1:3	HCl:DI		0:01:00			0:01:00
	437	Dump rinse 3x & dry	DI	N_2		0:01:30	0:01:00		0:01:00
HF Bench	438	Native oxide strip of **Si Monitor #6 (a-e)**	BHF			0:00:30		Prepare at least five Si monitors to check BCB spin speed	0:01:00
	439	Dump rinse 3x	DI			0:01:00			0:01:00

BCB Spin - 1:04									
PR Bench	440	Spin BCB solution on **Si Monitor #6**	*(dilute) 3022-46*	*4 krpm*	10 krpm/s	0:00:40	0:00:30	Dilute with 2 parts T1100 to 1 part 3022-46	0:01:00
Ellipsometer (JAW)	441	Measure **Si Monitor #6**	"Cauchy on Si"					d = ~300 nm; change speed and re-spin on new Si if necessary; spin w/ final spin speed on at least 3 samples for dry etching	0:01:00
	442	Check fit in Analysis	$\lambda > 350$ nm	$\lambda < 1600$ nm				Record thickness and refractive index @ {450 nm, 632.8nm}	0:01:00
PR Bench	443	Dehydration bake; let cool	180 °C			0:02:00	0:01:00		0:01:00
	444	Mount on blue tape							0:02:00
	445	Adsorb & spin adhesion promoter	AP3000	*4 krpm*	10 krpm/s	0:00:40	0:00:30	Use spin speed found for **Si Monitor #5**	0:01:00
	446	Unmount from tape							0:02:00
	447	Bake	180 °C			0:01:00			0:01:00
	448	Mount on blue tape							0:02:00
	449	Dispense **BCB**, dwell & spin, ***~300 n m***	*(dilute) 3022-46*	*4 krpm*	10 krpm/s	0:00:40	0:00:30	Use spin speed found for **Si Monitor #5**	0:01:00
	450	Unmount from tape							0:02:00
	451	Soft Bake	50-100-150 °C			0:45:00		ramp every 15 minutes on hotplate; minimizes blisters by heating from bottom (i.e. on hotplate)	0:01:00

Final Cure - 5:24									
Blue M Oven	452	Load sample and **Si Monitor #6 (a-e)**						use Al boat; DO NOT cover	0:01:00
	453	Close door; leave note							0:01:00
	454	Check N_2; reduce flow after time	N_2	60-70 %		0:03:00			0:01:00
	455	Run program 5:						Check that temp rises!	0:05:00
	456	- ramp, soak	50 °C	50 °C		0:05:00	0:05:00	time in program is 0.05 for 5 min	0:00:00
	457	- ramp, soak	100 °C	100 °C		0:15:00	0:15:00		0:00:00
	458	- ramp, soak	150 °C	150 °C		0:15:00	0:15:00		0:00:00
	459	- ramp, soak	250 °C	250 °C		1:00:00	1:00:00	time in program is 1.00 for 5 min	0:00:00
	460	cool down	<150 °C			2:00:00		Do not open door until cooled!	0:00:00
	461	Remove sample&monitor, turn off						Turn off N_2 as well	0:01:00
Ellipsometer (JAW)	462	Measure **Si Monitor #6**	"Cauchy on Si"					d = ~290 nm; make note of shrinkage after cure	0:01:00
	463	Check fit in Analysis	$\lambda > 350$ nm	$\lambda < 1600$ nm				Record thickness and refractive index @ {450 nm, 632.8nm}	0:01:00

p-Contact Lithography (LOL2000/SPR220-3.0) - 1:15									
Equipment	***ID #***	***Procedure***	***P1***	***P2***	***P3***	***T1***	***T2***	***Notes***	***T0***
Pre-Clean - 0:08									
Solvent Bench	464	Clean	Acetone	IPA		0:01:00	0:01:00	No sonication	0:01:00
	465	Dump rinse 3x	DI			0:01:00			0:01:00
	466	Add Liquinox; dump rinse 3x & dry	Liquinox	DI	N_2	0:01:00	0:01:00	1 squirt, then fill beaker with water	0:01:00
PR Spin - 0:00									
PR Bench	467	Dehydration bake	170 °C			0:02:00			0:02:00
	468	Mount sample on blue tape							0:05:00
	469	**Spin underlayer, Recipe #5: ~160 nm**	LOL2000	5 krpm	10 krpm/s	0:00:30			0:01:00
	470	Unmount; clean backside	EBR100						0:10:00
	471	Soft Bake	170 °C			0:05:00		Set dissolution rate: ~ 5 nm/sec	0:01:00
	472	Setup new wipes in spinner bowl						vapor will contaminate PR spin	0:01:00
	473	Mount sample on blue tape							0:05:00
	474	**Spin PR ~2.5 µm thick**	SPR220-3.0	5 krpm	10 krpm/s	0:00:30			0:02:00
	475	Unmount; clean backside	EBR100						0:10:00
	476	Soft bake	115 °C			0:01:30			0:01:00

Stepper Lithography - 0:52									
GCA AutoStep 200	477	Login						"L I [10,3]"	0:01:00
	478	Move robot to loading position						"RMSL"	0:01:00
	479	Load mask: "4B_PCONT-P"						load w/barcode in lower right corner	0:01:00
	480	Take inventory						<CR> after "RMSL", or "INV"	0:01:00
	481	Edit prgm EGCLD: COL/ROW	1 row	*7 col.*				# col. Based on width of sample ÷ 1.63 mm	0:02:00
	482	Edit prgm EGCLD: Alignment Keys	Right: R1C7	Left: R1C2					0:02:00
	483	Edit pass EGCLD\PCONT: barcode	~~PCONT-P~~ NONE					~~barcode corresponds to mask~~; THIS BARCODE IS INCORRECT, USE "NONE" AND ENTER FLOOR #	0:01:00
	484	Edit pass EGCLD\PCONT: pass shift	x = 0	y = 0					0:02:00
	485	Edit pass EGCLD\RIDGE: exposure, offset	0.65 sec	+0 offset					0:01:00
	486	Run "SETUP"							0:02:00
	487	Change chuck size in software	7100					"CHUCK" -> "C" -> "7100" -> "Q"	0:01:00
	488	Load chuck on stepper stage						turn on stage vacuum	0:01:00
	489	Run focus & expose passes						"EXEC EGCLD" -> "FOCUS, P-CONT"	0:01:00
	490	Align and expose	0.65 sec	+0 offset				align right key first, left key for theta	0:05:00
	491	Record voltages for manual focus						during "FOCUS" pass	0:05:00
	492	Switch to manual column height control						between "FOCUS" and "P-CONT" passes	0:01:00
	493	Set manual focus and expose each die						First die should fail; set focus before each die is exposed; For edge die, average the recorded value and its neighbor	0:05:00
	494	Abort and unload masks						"Ctrl + c -> a","RMSR", "RMSL", remove masks, <CR>	0:01:00
	495	Unload sample						"LOAD"; turn off stage & chuck vacuums	0:01:00
PR Bench	496	Let sample outgas				0:05:00			0:01:00
	497	Post Exposure Bake	115 °C			0:01:30			0:01:00
	498	Hard Bake	100 °C			0:10:00		Prevents drooping of SPR above undercut region	0:01:00

PR Develop - 0:15									
Develop Bench	499	**Develop**, checking undercut often	AZ300MIF			0:01:00	0:00:15	develop 15 sec after PR done to minimize undercut	0:01:00
	500	Dump rinse 3x & dry	DI	N_2		0:01:00	0:01:00		0:01:00
µscope	500	Inspect						Develop longer if necessary to clear pattern	0:05:00
Dektak	501	Dektak						Record step height.	0:05:00

p-Contact Dry Etch (BCB) - 4:19

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
PR Descum - 0:04									
PEII	502	**PR Descum: 20 nm**	300 mT	100 W		0:00:20		~1 nm/sec	0:04:00
BCB Dry Etch - 0:49									
ICP #2	503	Gas change: *SF_6 -> CF_4*				0:05:00		if necessary	0:03:00
	504	Etch test recipes: *109*				0:04:00	0:04:00	if necessary	0:03:00
	505	Clean & load O_2 cleaning wafer	Acetone	IPA	DI/N2			Clean & check backside	0:05:00
	506	O_2 clean, Recipe: 103	40 sccm	900/100 W	0.5 Pa	0:05:00			0:02:00
	507	Change recipe #126: "BCBVert" - CF_4/O_2 etch	10/40 sccm	500/0 W 500/0 W 500/100 W	2 Pa 1 Pa 0.2 Pa	0:00:02 0:00:03 0:05:00		Pressure drop needs to be controlled in order to prevent plasma flame out	0:01:00
	507	Clean & load seasoning wafer	Acetone	IPA	DI/N2			Clean & check backside	0:05:00
	508	CF_4/O_2 coat, use recipe #126	10/40 sccm	500/100 W	2 Pa	0:02:00		Change recipe, then change back later	0:02:00
	509	Clean & load etch carrier wafer w/sample	Acetone	IPA	DI/N2			Mount w/a little Santovac diffusion pump oil	0:05:00
	510	**~350 nm BCB etch**, #126	10/40 sccm	300/100 W	0.2 Pa	0:01:00		BCB etch rate ~ 350 nm/min	0:02:00
Inspect - 1:36									
µscope	511	Inspect; check that dielectric is visibile							0:01:00
SEM	512	Inspect; check ridge & grating	SEI @ 6 mm	LEI @ 11 mm	15 kV			SEI for material differences, LEI for topography	0:45:00
AFM	513	Inspect; check vertical ridge & deep grating						Isolate tip to the top of ridge with grating, scan 8 µm wide	0:45:00
Dektak	514	Dektak RIDGE pad						Record step height.	0:05:00
BCB Cleanup Dry Etch {IF NECESSARY} - 0:14									
ICP #2	515	If necessary, **~60 nm BCB etch**, #126	10/40 sccm	500/100 W	0.2 Pa	0:00:10		BCB etch rate ~ 350 nm/min	0:01:00
	515	Load O_2 cleaning wafer							0:01:00
	516	O_2 clean, Recipe: 103	40 sccm	900/100 W	0.5 Pa	0:05:00			0:02:00
	517	Unload carrier, unmount sample	Acetone	IPA	DI			careful not to scratch sample, PhC are fragile	0:05:00
Inspect {IF NECESSARY} - 1:36									
µscope	518	Inspect; check that dielectric is visibile							0:01:00
SEM	519	Inspect; check ridge & grating	SEI @ 6 mm	LEI @ 11 mm	15 kV			SEI for material diff., LEI for topography	0:45:00
AFM	520	Inspect; check for grating						Isolate tip to the top of ridge with grating	0:45:00
Dektak	521	Dektak RIDGE pad						Record step height.	0:05:00

p-Contact Deposition (Pd) & Lift-Off - 1:05

Equipment	*ID #*	*Procedure*	*P1*	*P2*	*P3*	*T1*	*T2*	*Notes*	*T0*
Oxide Wet Etch - 0:16									
PEII	522	**PR Descum: 20 nm**	300 mT	100 W		0:00:20		~1 nm/sec	0:04:00
HF Bench	523	Time BHF etch of Si Monitor #3, 400 nm	BHF			*0:01:20*	0:00:10	check if water beads up on monitor, record etch time Etch rate ~ 300 nm/min; Si Monitor #3 COMPLETE	0:01:00
	524	Etch sample, Si Monitor #6 & #7	BHF			*0:01:20*		Etch for same time as above	0:01:00
	525	Dump rinse 3x	DI			0:01:00			0:01:00
Dektak	526	Dektak						Record step height.	0:05:00
Metal Deposition - 0:19									
Ebeam 3	527	Tape sample to angled stage	23.6 °					Angle towards Gun 2 w/LD ridges perpendicular to tilt axis Use Kapton tape on GaN/Si to assist with lift-off	0:01:00
	528	**75 nm Pd** deposition	750 Å	1 Å/sec		*0:08:30*			0:05:00
µscope	529	Inspect deposition							0:05:00
Lift-Off - 0:30									
Solvent Bench	530	**Strip photoresist**, agitate w/pipette	Acetone			0:10:00		Do not use 1165 with BCB	0:01:00
	531	**Strip**, agitate w/pipette	Acetone	IPA		0:02:00	0:02:00		0:01:00
	532	Cascade Dump rinse 3x & dry	DI	N_2		0:02:00	0:01:00		0:01:00
µscope	533	Inspect, repeat strip if necessary							0:05:00
Dektak	534	Dektak RIDGE pad						Record step height.	0:05:00

Adhesion Layer Deposition (Si3N4) - 1:35

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
PR Descum - 0:04									
PEII	535	**PR Descum: 20 nm**	300 mT	100 W		0:00:20		~1 nm/sec	0:04:00
Si3N4 Deposition - 1:31									
Sputter 3	536	Load **Si Monitor #7**	gun ∠ = 9	h = 25	max rot.				0:05:00
	537	Backsputter and 50 nm Si3N4 dep, Recipe: "Nedy Si3N4_backsputter"	Gun/Bias = 200/10 W	Ar/N2 = 25/3 sccm	3 mTorr	0:01:00	0:32:15	backsputter clean at Bias = 100 W before dep; T2 calib.: ~ 1.55 nm/min	0:01:00
Ellipsometer (JAW)	538	Measure **Si Monitor #7**	"Cauchy on Si"						0:01:00
	539	Check fit in Analysis	λ > 350 nm	λ < 1600 nm				Record thickness and refractive index @ {450 nm, 632.8nm} and confirm that target is not worn out	0:01:00
Sputter 3	540	Load sample and **Si Monitor #8**	gun ∠ = 9	h = 25	max rot.				0:05:00
	541	Back sputter and **50 nm Si3N4** dep, Recipe: "Nedy Si3N4_backsputter"				0:01:00	*0:32:15*	backsputter clean at Bias = 100 W before dep; T2 calib.: ~ 1.55 nm/min	0:01:00
Ellipsometer (JAW)	542	Measure **Si Monitor #8**	"Cauchy on Si"						0:01:00
	543	Check fit in Analysis	λ > 350 nm	λ < 1600 nm				Record thickness and refractive index @ {450 nm, 6	0:05:00
µscope	544	Inspect						Visual check:	0:05:00

p-Via Lithography (SPR220-3.0) - 1:20

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
Pre-Clean - 0:12									
Solvent Bench	545	Clean	Acetone	IPA		0:01:00	0:01:00	No sonication	0:01:00
	546	Dump rinse 3x	DI			0:01:00			0:01:00
	547	Add Liquinox; dump rinse 3x & dry	Liquinox	DI	N_2	0:01:00	0:01:00	1 squirt, then fill beaker with water	0:01:00
PEII	548	**PR Descum: 20 nm**	300 mT	100 W		0:00:20		~1 nm/sec	0:04:00
PR Spin - 0:20									
PR Bench	549	Dehydration bake	115 °c			0:01:30			0:02:00
	550	Mount sample on blue tape							0:05:00
	551	**Spin PR ~2.5 µm thick**	SPR220-3.0	5 krpm	10 krpm/s	0:00:30			0:02:00
	552	Unmount; clean backside	EBR100						0:10:00
	553	Soft bake	115 °C			0:01:30			0:01:00

Stepper Lithography - 0:41									
GCA AutoStep 200	554	Login						"L I [10,3]"	0:01:00
	555	Move robot to loading position						"RMSL"	0:01:00
	556	Load mask: "4B_PCONT-P"						load w/barcode in lower right corner	0:01:00
	557	Take inventory						<CR> after "RMSL", or "INV"	0:01:00
	558	Edit prgm EGCLD: COL/ROW	1 row	*7 col.*				# col. Based on width of sample ÷ 1.63 mm	0:02:00
	559	Edit prgm EGCLD: Alignment Keys	Right: R1C7	Left: R1C2					0:02:00
	560	Edit pass EGCLD\PCONT: barcode	~~PCONT-P~~ NONE					~~barcode corresponds to mask~~; THIS BARCODE IS INCORRECT, USE "NONE" AND ENTER FLOOR #	0:01:00
	560	Edit pass EGCLD\PCONT: pass shift	x = 0	y = 0					0:02:00
	561	Edit pass EGCLD\RIDGE: exp., offset	0.65 sec	+0 offset					0:01:00
	562	Run "SETUP"							0:02:00
	563	Change chuck size in software	7100					"CHUCK" -> "C" -> "7100" -> "Q"	0:01:00
	564	Load chuck on stepper stage						turn on stage vacuum	0:01:00
	565	Run focus & expose passes						"EXEC EGCLD" -> "FOCUS, P-VIA"	0:01:00
	566	Align and expose	0.65 sec	+0 offset				align right key first, left key for theta	0:05:00
	567	Record voltages for manual focus						during "FOCUS" pass	0:05:00
	568	Switch to manual column height control						between "FOCUS" and "P-VIA" passes	0:01:00
	569	Set manual focus and expose each die						First die should fail; set focus before each die is exposed; For edge die, average the recorded value and its neighbor	0:05:00
	570	Abort and unload masks						"Ctrl + c -> a","RMSR", "RMSL", remove masks, <CR>	0:01:00
	571	Unload sample						"LOAD"; turn off stage & chuck vacuums	0:01:00
PR Bench	572	Let sample outgas				0:05:00			0:01:00
	573	Post Exposure Bake	115 °C			0:01:30			0:01:00

PR Develop - 0:07									
Develop Bench	574	**Develop**	AZ300 MIF			0:01:00			0:01:00
µscope	575	Inspect							0:05:00

p-Via Dry Etch (Si3N4) - 2:47

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
PR Descum - 0:04									
PEII	576	**PR Descum: 20 nm**	300 mT	100 W		0:00:20		~1 nm/sec	0:04:00
Si3N4 Dry Etch - 0:46									
ICP #2	577	Gas change: *SF_6 -> CF_4*				0:05:00		if necessary	0:03:00
	578	Etch test recipes: *109*				0:04:00	0:04:00	if necessary	0:03:00
	579	Clean & load O_2 cleaning wafer	Acetone	IPA	DI/N2			Clean & check backside	0:05:00
	580	O_2 clean, Recipe: 103	40 sccm	900/100 W	0.5 Pa	0:05:00			0:02:00
	581	Change recipe #126: "DielNano" - CF_4 etch	40 sccm	900/0 W 900/0 W 900/50 W	2 Pa 1 Pa 0.5 Pa	0:00:02 0:00:03 0:00:25		SiO2 etch rate = 120 nm/min SiNx etch rate = (> 100 nm/min) Al2O3 etch rate = BCB etch rate = GaN etch rate = 14 nm/min; d ~ 5 nm	0:01:00
	582	Clean & load seasoning wafer	Acetone	IPA	DI/N2			Clean & check backside	0:05:00
	583	CF_4 coat, use recipe #126	40 sccm	900/50 W	0.5 Pa	0:00:20			0:02:00
	584	Clean & load etch carrier wafer w/sample	Acetone	IPA	DI/N2			Mount w/a little Santovac diffusion pump oil	0:05:00
	585	**50 nm Si3N4 etch**, #126	40 sccm	300/100 W	0.2 Pa	0:00:20		BCB etch rate ~ 350 nm/min	0:02:00
Inspect - 1:31									
µscope	586	Inspect; check that dielectric is visibile							0:01:00
SEM	587	Inspect; check ridge & grating	SEI @ 6 mm	LEI @ 11 mm	15/4 kV			SEI for material diffs. - check for disruption of Pd surface; LEI for topography - Pd texture should be visible	0:45:00
AFM	588	Inspect; check vertical ridge & grating						Isolate tip to the top of ridge with grating, scan 8 µm wide	0:45:00
PR Strip - 0:25									
Solvent Bench	589	**Strip photoresist**, agitate w/pipette	Acetone			0:10:00		Do not use 1165 with BCB	0:01:00
	590	**Strip**, agitate w/pipette	Acetone	IPA		0:02:00	0:02:00		0:01:00
	591	Cascade Dump rinse 3x & dry	DI	N_2		0:02:00	0:01:00		0:01:00
µscope	592	Inspect, repeat strip if necessary							0:05:00

p-Pad Lithography (SF15/NR9-3000PY) - 1:26									
Equipment	***ID #***	***Procedure***	***P1***	***P2***	***P3***	***T1***	***T2***	***Notes***	***T0***
Pre-Clean - 0:08									
Solvent Bench	593	Clean	Acetone	IPA		0:01:00	0:01:00	No sonication	0:01:00
	594	Dump rinse 3x	DI			0:01:00			0:01:00
	595	Add Liquinox; dump rinse 3x & dry	Liquinox	DI	N_2	0:01:00	0:01:00	1 squirt, then fill beaker with water	0:01:00
PR Spin - 0:14									
PR Bench	596	Dehydration bake	170 °C			0:02:00			0:02:00
	597	Mount GaN on blue tape						corral with DSP sapphire in spiral pattern	0:05:00
	598	**Spin underlayer: 1900 nm thick**	SF15	5 krpm	10 krpm/s	0:00:30			0:01:00
	599	Unmount; clean backside	EBR100						0:10:00
	600	Soft bake - fast develop	170 °C			0:02:00		fast develop rate: 8 nm/sec	0:01:00
	601	Mount GaN on blue tape							0:05:00
	602	Dehydration bake; let cool	115 °C			0:02:00	0:01:00		0:01:00
	603	Mount on blue tape							0:02:00
	604	**Spin PR 2.233 µm thick**	NR9-3000PY	5 krpm	10 krpm/s	0:00:30			0:01:00
	605	Unmount; clean backside	EBR100						0:01:00
	606	Softbake	115 °C			0:05:00		Use lid (PR very sensitive to temp.)	0:01:00

Stepper Lithography - 0:44									
GCA AutoStep 200	607	Login						"L I [10,3]"	0:01:00
	608	Move robot to loading position						"RMSL"	0:01:00
	609	Load mask: "5B_PPAD-N"						load w/barcode in lower right corner	0:01:00
	610	Take inventory						<CR> after "RMSL", or "INV"	0:01:00
	611	Edit prgm EGCLD: COL/ROW	1 row	*7 col.*				# col. Based on width of sample ÷ 1.63 mm	0:02:00
	612	Edit prgm EGCLD: Alignment Keys	Right: R1C7	Left: R1C2					0:02:00
	613	Edit pass EGCLD\P-PAD: barcode	PPAD-N					barcode corresponds to mask	0:01:00
	613	Edit pass EGCLD\P-PAD: pass shift	x = 0	y = 0					0:02:00
	614	Edit pass EGCLD\RIDGE: exp., offset	0.79 sec	-16 offset					0:01:00
	615	Run "SETUP"							0:02:00
	616	Change chuck size in software	7100					"CHUCK" -> "C" -> "7100" -> "Q"	0:01:00
	617	Load chuck on stepper stage						turn on stage vacuum	0:01:00
	618	Run focus & expose passes						"EXEC EGCLD" -> "FOCUS, PPAD"	0:01:00
	619	Align and expose	0.79 sec	-16 offset				align right key first, left key for theta	0:05:00
	620	Record voltages for manual focus							0:01:00
	621	Switch to manual column height control						For edge die, average the recorded value and its nei	0:01:00
	622	Abort and unload masks						"Ctrl + c -> a","RMSR", "RMSL", remove masks, <CR>	0:01:00
	623	Unload sample						"LOAD"; turn off stage & chuck vacuums	0:01:00
PR Bench	624	Let sample outgas				0:05:00			0:01:00
	625	Post Exposure Bake	115 °C			0:02:00		Use lid (PR very sensitive to temp.)	0:01:00
	626	Hard Bake	100 °C			0:10:00		Prevents PR from drooping	0:01:00

PR Develop - 0:19									
Develop Bench	627	**Develop PR**	AZ300 MIF			0:00:40		PR develops very fast (~11 s), over develop for slight undercut;	0:01:00
DUV Flood Expose	628	Flood expose SF15	max rotation			0:05:00			0:01:00
Develop Bench	629	**Develop underlayer**	101A			0:01:00			0:01:00
µscope	630	Inspect						check undercut	0:05:00
Dektak	631	NO DEKTAK						Dektak will tear PR	0:05:00

p-Pad Deposition (Ti/Ni/Au) & Lift-Off - 3:43

Equipment	*ID #*	*Procedure*	*P1*	*P2*	*P3*	*T1*	*T2*	*Notes*	*T0*
PR Descum - 0:04									
PEII	632	**PR Descum: 20 nm**	300 mT	100 W		0:00:20		~1 nm/sec	0:04:00
Metal Deposition - 1:07									
E-beam #3	633	Load sample and **Si Monitor #5** at an angle	23.6 °					Angle towards Gun 1 w/ LD ridges perpendicular to tilt axis; use Kapton tape on GaN to assist with lift-off and on Si to create a dektak mark	0:15:00
	634	**35/35 nm Ti/Ni** Deposition	350/350 Å	1-2-4 Å/sec		*0:02:00*			0:15:00
	635	**1 µm Au** Deposition	10 kÅ	1-3-5 Å/sec		*0:30:00*			0:05:00
Lift-Off - 0:18									
Solvent Bench	636	**Strip photoresist**, agitate w/pipette; soak	Acetone			0:10:00		Avoid 1165 with BCB; soak upside down	0:01:00
	637	**Strip**, agitate w/pipette	Acetone	IPA		0:02:00	2:00:00	Use fresh beaker; do not allow acetone to dry on sa	0:01:00
Develop Bench	638	Dump rinse 3x	DI			0:01:30			0:01:00
	639	**Strip underlayer**	AZ300 MIF			0:02:00			0:01:00
	640	Add Liquinox; dump rinse 3x & dry	Liquinox	DI	N_2	0:01:00	0:01:00	1 squirt, then fill beaker with water	0:01:00
µscope	641	Inspect: complete LO						Repeate LO if necessary	0:05:00
Dektak	642	Dektak RIDGE pad						Record step height.	0:05:00

n-Via Lithography (SPR220-7.0) - 0:50									
Equipment	***ID #***	***Procedure***	***P1***	***P2***	***P3***	***T1***	***T2***	***Notes***	***T0***
Pre-Clean - 0:08									
Solvent Bench	643	Clean	Acetone	IPA		0:01:00	0:01:00	No sonication	0:01:00
	644	Dump rinse 3x	DI			0:01:00			0:01:00
	645	Add Liquinox; dump rinse 3x & dry	Liquinox	DI	N_2	0:01:00	0:01:00	1 squirt, then fill beaker with water	0:01:00
PR Spin - 0:20									
PR Bench	646	Dehydration bake	115 °c			0:01:30			0:02:00
	647	Mount sample on blue tape							0:05:00
	648	**Spin PR ~5.5 µm thick**	SPR220-7.0	5 krpm	10 krpm/s	0:00:30			0:02:00
	649	Unmount; clean backside	EBR100						0:10:00
	650	Soft bake	115 °C			0:01:30			0:01:00
Stepper Lithography - 0:14									
Contact Aligner	651	Mask sample with Al foil						Leave one side of Si carrier exposed; GaN fully covered	0:01:00
	652	Flood expose				0:01:00			0:01:00
	653	Mask sample with Al foil						Leave other side of Si carrier exposed	0:01:00
	654	Flood expose				0:01:00			0:01:00
	655	Outgas				0:10:00			0:01:00
PR Develop - 0:08									
Develop Bench	642	**Develop**	AZ300 MIF			0:02:30			0:01:00
µscope	643	Inspect							0:05:00

n-Via Dry Etch (BCB/Si3N4/SiO2) - 1:38

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
PR Descum - 0:05									
PEII	656	**PR Descum: 20 nm**	300 mT	100 W		0:01:00		~1 nm/sec	0:04:00
Dielectrics Dry Etch - 1:07									
ICP #2	657	Gas change: *SF_6 -> CF_4*				0:05:00		if necessary	0:03:00
	658	Etch test recipes: *109*				0:04:00	0:04:00	if necessary	0:03:00
	659	Clean & load O_2 cleaning wafer	Acetone	IPA	DI/N2			Clean & check backside	0:05:00
	660	O_2 clean, Recipe: 103	40 sccm	900/100 W	0.5 Pa	0:05:00			0:02:00
	661	Change recipe #126: "BCBVert" - CF_4/O_2 etch	10/40 sccm	500/0 W 500/0 W 500/100 W	2 Pa 1 Pa 0.2 Pa	0:00:02 0:00:03 0:02:00		Pressure drop needs to be controlled in order to prevent plasma flame out	0:01:00
	662	Load carrier wafer w/sample and etch: #126	10/40 sccm	500/100 W	0.2 Pa	0:02:00			0:05:00
	661	Change recipe #126: "DielNano" - CF_4 etch	40 sccm	900/0 W 900/0 W 900/50 W	2 Pa 1 Pa 0.5 Pa	0:00:02 0:00:03 0:04:00			0:01:00
	663	Load carrier wafer w/sample and etch: #126	40 sccm	900/50 W	0.5 Pa	0:04:00			0:05:00
	664	Change recipe #126: "BCBVert" - CF_4/O_2 etch	10/40 sccm	500/0 W 500/0 W 500/100 W	2 Pa 1 Pa 0.2 Pa	0:00:02 0:00:03 0:02:00		Pressure drop needs to be controlled in order to prevent plasma flame out	0:01:00
	665	Load carrier wafer w/sample and etch: #126	10/40 sccm	500/100 W	0.2 Pa	0:02:00			0:05:00
	666	Change recipe #126: "DielNano" - CF_4 etch	40 sccm	900/0 W 900/0 W 900/50 W	2 Pa 1 Pa 0.5 Pa	0:00:02 0:00:03 0:00:25			0:01:00
	667	Load carrier wafer w/sample and etch: #126	40 sccm	900/50 W	0.5 Pa	0:04:00			0:05:00
Inspect - 0:01									
µscope	668	Inspect; check that Si is cleared of dielectics						Repeat dry etch if necessary	0:01:00
PR Strip - 0:25									
Solvent Bench	669	**Strip photoresist**, agitate w/pipette	Acetone			0:10:00		Do not use 1165 with BCB	0:01:00
	670	**Strip**, agitate w/pipette	Acetone	IPA		0:02:00	0:02:00		0:01:00
	671	Cascade Dump rinse 3x & dry	DI	N_2		0:02:00	0:01:00		0:01:00
µscope	672	Inspect, repeat strip if necessary							0:05:00

Dice LDs - 1:37

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
Attach Coverslip - 0:33									
Dicing Saw	673	Retrieve a thin, 4" unpolished Si wafer	~265 µm					For use as a dicing carrier wafer	0:01:00
	674	Drop gauge carrier wafer						Record value + "tape thickness" = WH thickness + 0.02	0:01:00
Solvent Bench	674	Cleave coverslip to approx. size of GaN	#1, ~145 µm					Make sure diced coverslip can cover entire GaN sample	0:01:00
	675	Cleave dummy Si piece						Slightly larger than cleaved coverslip	0:01:00
	676	Clean sample, coverslip, dummy and 4" wafer	Acetone	IPA		0:01:00	0:01:00	No sonication	0:01:00
	677	Dump rinse 3x	DI			0:01:00			0:01:00
	678	Add Liquinox; dump rinse 3x & dry	Liquinox	DI	N_2	0:01:00	0:01:00	1 squirt, then fill beaker with water	0:01:00
	679	Mount sample on blue tape, upside down							0:01:00
	680	**Spin dissolved wax** on backside, Prgm #49	Crystal Bond in acetone	0.5 krpm	0.5 krpm/sec	0:01:15		Only use left solvent bench spin coater; use syringe & filter; 40 g Crystal bond dissolved in 200 mL acetone	0:01:00
	681	Unmount sample							0:01:00
	682	Mount coverslip on blue tape							0:01:00
	683	**Spin dissolved wax** on coverslip, Prgm #49	Crystal Bond in acetone	0.5 krpm	0.5 krpm/sec	0:01:15		Only use left solvent bench spin coater; use syringe & filter; 40 g Crystal bond dissolved in 200 mL acetone	0:01:00
	684	Unmount coverslip							0:01:00
	685	Change back to Prgm #1						Prevents #49 from being edited	0:01:00
PR Bench	685	Bake coverslip & sample, wax face up	110 °C			0:00:30		Place both on Si standoffs so GaN/wax doesn't touch hot plate	0:01:00
	686	Melt crystal bond chunks in Al cup	110 °C			0:00:30			0:01:00
	686	Scrape Al cup with razor blade						Creates thin lines of wax on edge	0:01:00
	686	Stack coverslip on sample on 4" carrier						Wax face down; make sure coverslip covers GaN completely	0:01:00
	686	Place thin lines of wax next to coverslip						Place on left and right sides - wicks underneath when heated; Along with 4" carrier, helps to reduce vibration during dicing	0:01:00
	687	Bake stack	110 °C						0:01:00

Vacuum Bonder	688	Turn on, unscrew locking pin, open carefully						Switch on right side; quartz base may stick to upper	0:01:00
	689	Clean upper membrane	IPA					Do not use acetone!	0:01:00
	690	Place sample on base							0:01:00
	691	Cut 1" square wipes and stack (2) on top							0:01:00
	691	Stack the Si dummy piece on sample						Prevents the coverslip from shattering	0:01:00
	692	Cut 4" circle wipes and stack (2) on top							0:01:00
	693	Close and tighten locking pin						2 finger tight!	0:01:00
	694	Set pressure	10 psi						0:01:00
	695	Program recipe	Start: 110°C End: 60°C	Proceed: 25 mBar	Abort: 32 mBar	0:05:00 0:10:00	0:10:00 0:01:00	Process Control: Heat & Outgas; Times: soak & bond (T1), out gass & P.P. del (T2)	0:01:00
	696	Run: "Process" -> "Start"				0:15:00		If program aborts twice, the o-ring is leaking	0:11:00
	697	Unscrew locking pin and open carefully						Sample base may stick to upper membrane	0:01:00
	698	Remove sample and wipes							0:01:00
	699	Clean upper membrane	IPA					Do not use acetone!	0:01:00

Dice LD Bars - 1:03									
	700	Login w/username & password	speck	speck					0:01:00
	701	System init							0:03:00
	702	Change blade and flange	R07-SD400-BB200-50	blade dim.: 55.5x0.2xA2x40	52 mm			200 µm wide resin blade with 400 grit (23 µm?); produces ~215 µm wide streets with chips ~20 µm	0:05:00
	703	Drop gauge 4" carrier, 1" carrier, and stack						Record values	0:01:00
	703	Attach UV tape to mounting frame						Cut tape and remove frame *without* sample!	0:01:00
	704	Mount 4" carrier & sample on tape						Use razor blade to pop air bubbles on back side	0:01:00
	705	Load frame and sample							0:01:00
	706	Check recipe: "Nedy - GaN on Si LDs" - main	R07-SD400-BB200-50	tape ~ 0.35	wafer ~ 1			Make sure selected blade matches in recipe: 2.187-4C-30RU-3; tape thickness = 0.09 + 4" carrier; wafer thickness = stack - 4" carrier	0:01:00
	707	Check recipe: "Nedy - GaN on Si LDs"	35 krpm 0.5 mm/sec	d ~ 0.38 mm l = 45.4 mm	overtravel 10 mm			At least 8.5 mm overtravel required for a 1 mm stack	0:01:00
	707	Define job: "Nedy - GaN on Si LDs"						Dress cuts in the Si only: 4 cuts in 2 steps	0:01:00
Dicing Saw	708	Align rotation using dice marks on GaN						May need to change focus: increase z by 0.15 mm;	0:01:00
	709	Define 0/1 cut using Si carrier	(0,0) mm					Zero y to top of GaN 900um LD bar, x to right edge of Si carrier	0:01:00
	710	Define 0/2 cut using Si carrier	(0,1.5) mm						0:01:00
	711	Run y offset alignment twice on 4" carrier	(0,30) mm	(0,-30) mm					0:01:00
	712	Run y offset alignment twice on 1" Si	(0,5) mm	(0,-5) mm				Cut 5 mm from Si edges; make sure sample & cover	0:05:00
	713	Check cut map for all cuts	(15,0) mm	(I) mode				Make sure cuts are aligned to GaN dice marks	0:01:00
	714	Re-select step 0/1						Dicer will start on currently selected step!	0:01:00
	715	Run full wafer cut	35 krpm 0.5 mm/sec	d ~ 0.38 mm l = 45.4 mm	overtravel 10 mm	*0:10:00*			0:10:00
	716	"Wafer Unload"; clean & unload sample	DI	N_2		0:01:00	0:01:00	Remove as much dust as possible before unloading; Careful! Do not get too close to sample - 6" away	0:01:00
	717	Load and run UV curing station				0:01:30			0:01:00
	718	Unload blade							0:05:00
	719	Cut UV tape around Si carrier						Cut out and store on tape in fluoroware	0:01:00
µscope	720	Inspect dicing						Take pictures of diced facets; measure and record c	0:05:00

Polish 1st LD Bar - 21:00

Equipment	ID #	Procedure	P1	P2	P3	T1	T2	Notes	T0
Clean & Setup - 0:13									
Polisher Hood	721	Open water supply line							0:01:00
	722	Clean crystal bond off surfaces *thoroughly* with wipes and q-tips	Acetone					Chuck (top and bottom), hotplate, cooling block, polisher spindle arm mounting pin & surface... any suface chuck touches	0:10:00
	723	Turn on hot plate and set temp	150 °C						0:01:00
Drop Gauge	724	Check that chuck is flat at 4 pts around edge	< Δ2 µm					Move gauge manually (don't use plunger)	0:01:00
Level Polisher - 0:35									
Polisher	725	Detach spindle arm, move aside							0:01:00
	726	Clean and mount platen on polisher						Clean groove on platen backside & matching polisher surface Match the "A" peg with the "A" hole	0:01:00
	727	Re-attach spindle arm and adjust sweep	Oscillation					check that edge of chuck does not sweep past center or edge of the platen	0:01:00
	728	Move spindle arm to middle of sweep	Oscillation						0:01:00
	729	Clamp µmeter to holder to spindle arm						µmeter should point down to touch platen	0:01:00
	730	Set downward force	600 g = "Full"						0:01:00
	731	Position spindle arm at half-radius of platen	Oscillation						0:01:00
	732	Lower cam on spindle arm							0:01:00
	733	Lower spindle arm and zero µmeter						Check µmeter has enough range of motion, then ze	0:01:00
	734	Rotate spindle arm, measure leveling	Full Rotation					if deviation > 20 ticks, follow polisher manual to level spindle	0:01:00
	735	Raise spindle arm then cam, remove µmeter							0:01:00
	736	Clamp chuck to spindle arm							0:01:00
	737	Afix µmeter to platen to measure chuck						Use double-sided tape; align measurement end w/	0:01:00
	738	Lower cam on spindle arm							0:01:00
	739	Lower the spindle arm on to µmeter						Check µmeter has enough range of motion, then ze	0:01:00
	740	Rotate chuck until µmeter stops drifiting				0:02:00		"Full Rotation"; wait at least T1; should settle into a	0:01:00
	741	Rotate chuck to align screw						The screw is btw the two µpositioners; "µp-A" is CW	0:01:00
	742	Re-adjust spindle arm						To zero µmeter; check µmeter has enough range of	0:01:00
	743	Rotate chuck until µmeter stops drifiting						"Full Rotation"; should settle into a repeated oscilla	0:01:00
	744	Rotate chuck to µp-A, check µmeter						Should read zero- else zero w/spindle & repeat last	0:01:00
	745	Rotate chuck to half way to µp-B and zero						Zero µmeter using µp-B	0:01:00
	746	Check µmeter at screw -> µp-A -> µp-B						Leveling ±1 tick of µmeter gauge = 2 µm across chuc	0:01:00
	747	Rotate chuck, check & repeat alignment						Should read zero, else repeat alignments *in the sam*	0:10:00
	748	Raise spindle arm, then raise cam							0:01:00
	749	Remove µmeter and chuck							0:01:00

Mount LD Bar - 0:24									
µscope	750	Inspect facets of a chosen LD bar						Take (6) pictures of diced edges: center, left, right of each	0:05:00
	751	Find side that is parallel to intended facets						Polish opposite side 1st; record length req. to polish at centers	0:05:00
Polisher Hood	752	Heat sample on hotplate, remove LD bars	150 °C					Remove 1" Si carrier (and stack) from 4" Si carrier	0:01:00
	753	Heat chuck on hotplate, face up	150 °C						0:01:00
	754	Melt crystal bond on chuck						Use a generous amount, then scrape flat with a razo	0:01:00
	755	Place 2 clamping Si pieces on chuck						Choose thickness based on LD bar height: 1/2 * h < t < h; Orient perpendicular to bottom groove, above & below center	0:01:00
	756	Place sample on chuck, 1st facet facing up						Top of sample facing away from groove on chuck bo	0:01:00
	757	Use tweezers to squeeze Si clamps						Si-GaN-coverslip stack sticks up between Si clamps;	0:01:00
	758	Use wooden Q-tips to push sample down						Keep Si clamps in place with tweezers	0:01:00
	759	Use swab to remove excess crystal bond						Keep Si clamps in place with tweezers; wipe top&sid	0:01:00
	760	Move chuck to cooling block				0:05:00		Chuck is hot, but can be gripped and moved quickly	0:01:00
µscope	761	At 50x, check µscope focus knob						If focus deviates > 20 ticks btw center/left/right, redo mounting	0:05:00
	762	Measure crystal bond gap, take pictures						Gap < 10 µm, else redo; center/left/right pics of diced edge, as well as significant chips from dicing	0:05:00
Drop Gauge	763	Zero drop gauge on sample center						Move gauge manually (don't use plunger)	0:01:00

Polish LD 1st Facet - 2:36									
Polisher	764	Set downward force	100 g = "1"						0:01:00
	765	Position nozzle and turn on water						Position nozzle midway btw center and left edge of platen	0:01:00
	766	Set platen rotation, turn on to spread water	60 rpm	CCW				Green button; spread water; red button to turn all off	0:01:00
	767	Place large grit film on platen	30 µm	diamond	non-PSA			Use new polish film for every LD bar; smooth side of film down	0:01:00
	768	Squeegee air & water bubbles from film						Test film adhesion to platen with fingers	0:01:00
	769	Turn on water & platen rotation, test film						Test film adhesion to platen with squeegee	0:01:00
	770	All off; mount chuck on spindle arm						Check that chuck is flush and flat; twist locking cam back	0:01:00
	771	Rotate chuck & set limit rotation magnets	Full Rotation	Limit Rotation	45°			rotate so top of sample faces out & parallel to platen radius; limit between ± 22.5°	0:01:00
	772	All stop; lower cam slowly						sample should not touch film	0:01:00
	773	Turn on limit rot., allow µmeter to settle	Limit Rotation					*Always* allow spindle arm µmeter to settle; zero if necessary	0:01:00
	774	Turn off rotation	Limit Rotation						0:01:00
	775	Turn spindle up/down until touching	200 µm					Carefully touch sample down, then increase to P1	0:01:00
	776	Raise spindle arm	raise 5 turns						0:01:00
	777	Turn on limit rot., allow µmeter to settle	Limit Rotation					*Always* allow spindle arm µmeter to settle; zero if necessary	0:01:00
	778	Turn on water and platen rotation	60 rpm	CCW					0:01:00
	779	Fold wipe and hold against polishing film						Meant to clean film *during* polishing; use new wipe every time	0:01:00
	780	Slowly lower spindle arm to clear off wax	CCW 5 turns			0:00:05			0:01:00
	781	Raise spindle, all stop	CW 5 turns						0:01:00
	782	Raise cam, carefully remove chuck							0:01:00
Polisher Hood	783	Dry sample, then use wet swab	N2	IPA	N2			Swab from center to edge in both directions	0:05:00
µscope	784	At 50x, check µscope focus knob						If focus deviates > 40 ticks btw center/left/right, redo mounting	0:05:00
	785	Measure crystal bond gap, take pictures						Gap < 10 µm, else redo; center/left/right pics of diced edge, as well as significant chips from dicing	0:05:00
Drop Gauge	786	Re-zero drop gauge on sample center						Move gauge manually (don't use plunger); should not differ	0:01:00

Polisher	787	Set downward force	300 g = "3"						0:01:00
	788	Mount chuck on spindle arm						Check that chuck is flush and flat; twist locking cam back	0:01:00
	789	Turn on limit rot., allow µmeter to settle	Limit Rotation					*Always* allow spindle arm µmeter to settle; zero if necessary	0:01:00
	790	Turn on: water, platen, oscillation	Oscillate						0:02:00
	791	Fold wipe and hold against polishing film						Meant to clean film *during* polishing; use new wipe every time	0:01:00
	792	Slowly lower spindle arm until µmeter reads ~200 µm and polish	lower ~5 turns	start: ~200 µm end: ~100 µm	remaining: 100 µm			Polish 1/2 dist. to facet as measured by spindle arm µmeter; Count and record the number of spindle arm oscilations	0:05:00
	793	Raise arm, all stop	CW 5 turns						0:01:00
	794	Raise cam, carefully remove chuck							0:01:00
Polisher Hood	795	Dry sample, then use wet swab	N2	IPA	N2			Swab from center to edge in both directions	0:05:00
Drop Gauge	796	Measure sample center						Move gauge manually (don't use plunger); compare to µscope measurement below	0:01:00
µscope	797	Measure proximity to ridge in µscope using paired Au markings (visible every 1.63 mm)						@ 150-30 µm to facet: dist. btw markings is 1/3 dist. from facet @ 30-0 µm to facet: dist. btw markings is 2x dist. from facet @ past facet: three markings visible - 5 µm tolerance	0:10:00
Polisher	798	Turn on limit rotation	Limit Rotation					*Always* allow spindle arm µmeter to settle; zero if necessary	0:01:00
	799	Mount chuck, polish w/ osc. & limit rot.	Oscillate CCW ~5 turns	start: 200 µm end: ~150 µm	remaining: 50 µm			Use wipe; repeat polishing steps until 50 µm to facet remain	0:05:00
Polisher Hood	800	Dry sample, then use wet swab	N2	IPA	N2			Swab from center to edge in both directions	0:05:00
Drop Gauge	801	Unmount chuck, measure sample center						Move gauge manually (don't use plunger); compare to µscope measurement below	0:03:00
µscope	802	Measure&record proximity to ridge in µscope using paired Au markings (every 1.63 mm)						@ 150-30 µm to facet: dist. btw markings is 1/3 dist. from facet @ 30-0 µm to facet: dist. btw markings is 2x dist. from facet @ past facet: three markings visible - 5 µm tolerance	0:10:00

Polisher	803	Set downward force	600 g = "Full"					Polish quickly and precisely - slow polishing is alway	0:01:00
	804	Remove polishing film, hang to dry						Stick to side of polisher to drip dry	0:01:00
	805	Replace film with finer diamond grit and repeat polishing with limit rot. & osc.	Limit Rotation Oscillate	6 µm diamond 20 µm, twice	3 µm diamond 5 µm, twice			use new film for every LD bar and new wipe every time; polish half distance at first and measure&record for each film;	0:40:00
	806	Rotate chuck & check limit rotation magnets	Full Rotation	Limit Rotation	45°			rotate so top of sample faces out; limit between ± 22.5°	0:01:00
	807	Replace film with finer diamond grit and repeat polishing with limit rotation only	Limit Rotation (don't oscillate)	1 µm diamond	1 µm			*P3* = distance remaining to facet; use new polish area or film for each facet; new wipe ea. time polish half distance at first and measure&record for each film; this is the riskiest step! If spindle arm µmeter stops measuring removal, stop and inspect in µscope- if "brown scum" appears on Si under µscope, use new polish area or film for 1 µm grit	0:20:00
	808	Replace film with finer AlOx grit and repeat polishing with limit rotation	Limit Rotation (don't oscillate)	300 nm AlOx twice	final polish twice	0:00:25	0:00:15	use new polish area or film for every facet; new wipe ea. time measure & record same as other films; use new polish area or film for every facet	0:05:00

Polish 2nd Facet & Cleanup - 2:35									
Polisher Hood	809	Heat chuck, remove sample	150 °C						0:01:00
	810	Repeat "Mount LD Bar" for 2nd facet							0:20:00
Polisher	811	Repeat polishing for 2nd facet							2:00:00
Polisher Hood	812	Heat chuck, remove sample	150 °C						0:01:00
	813	Scrape chuck with razor blade						Remove as much crystal bond as possible	0:01:00
	814	Turn off hotplate							0:01:00
	815	Move chuck to cooling block				0:05:00			0:01:00
	816	Thoroughly clean & dry polisher							0:01:00
	817	Clean chuck, hotplate and cooling block	Acetone						0:01:00
	818	Turn off µscope light							0:01:00
	819	Close fume hood							0:01:00
	820	Close water supply line							0:01:00

Remove Coverslip - 0:25									
Solvent Bench	821	**Etch Crystal Bond**, agitate w/pipette	Acetone			0:10:00		Do not use 1165 with BCB	0:01:00
	822	**Remove Strip**, agitate w/pipette	Acetone	IPA		0:02:00	0:02:00	Use fresh beaker of acetone	0:01:00
	823	Cascade Dump rinse 3x & dry	DI	N_2		0:02:00	0:01:00		0:01:00
µscope	824	Inspect, repeat Ace & IPA if necessary						Take pictures of diced facets, confirm polishing distance & facets	0:05:00

Polish remaining LD Bars - 14:00									
Polisher	825	Repeat polishing on remaining LD bars							14:00:00